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RADIO RECEIVER
[musen jushin sochi]

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[Claims] /2*

[Claim 1] A radio receiver that has an amplifying means for receiving and amplifying high-frequency signals modulated by digital and analog signals, a reference signal generation means that generates a reference signal at a frequency almost equal to the center frequency of said high-frequency signals, a phase shift means that generates first and second reference signals whose phases intersect each other from said reference signal, a frequency conversion means that converts a frequency using the output signal of said amplifying means and said first and second reference signals, a baseband processing means that removes unnecessary frequency components from the output signals of said frequency conversion means and amplifies a desired signal, and a demodulation means that demodulates the output signals of the baseband processing means,

said radio receiver is also characterized by being equipped with an electric field strength measurement means that measures the electric field strength of said high-frequency signals as well as changes the signal amplification factor of said amplifying means, said frequency conversion means, and said baseband processing means in response to the electric field strength of the high-frequency signals.

[Claim 2] A radio receiver characterized by a radio communication system that transmits high-frequency signals modulated

* Claim and paragraph numbers correspond to those in the foreign text.

by digital signals or analog signals wherein a receiver is provided with one or a plurality of high-frequency amplifiers for amplifying said high-frequency signals, a local oscillator that generates a reference signal at a frequency almost equal to the center frequency of said high-frequency signals, a phase shift means for acquiring first and second reference signals whose phases intersect each other from the reference signal from said local oscillator, a first and a second frequency converter that multiplies said high-frequency signals and both first and second reference signals from said local oscillator and obtains a first and a second baseband signal, a first and second variable gain baseband circuit that takes the signals output from said frequency converter as input signals and then provides a gain to said input signals, a demodulator for demodulating the output signals of said baseband circuit, and a received power measurement circuit that measures the electric field strength of received signals,

said radio receiver is also characterized by being equipped with a function that varies the gain of at least one from among said high-frequency amplifier and said frequency converter, as well as a means that varies at least the gain of said baseband circuit and the gain of at least one from among the high-frequency amplifier and said frequency converter using control signals generated based on the received electric field strength measured by means of said received electric field strength measurement circuit.

[Claim 3] A radio receiver as set forth in Claim 2 characterized by said plurality of high-frequency amplifiers being comprised by a initial stage fixed gain amplifier and at least one or a plurality of latter stage variable gain amplifiers.

[Claim 4] A radio receiver as set forth in Claim 2 or Claim 3 characterized by the gain of said baseband circuit being continuously varied using control signals generated based on the received electric field strength measured by means of said received electric field strength measurement circuit.

[Claim 5] A radio receiver as set forth in Claim 2 characterized by being equipped with a means that varies the gain of a high-frequency amplifier and a high frequency converter in steps using control signals generated based on the received electric field strength measured by means of said received electric field strength measurement circuit and then continuously varies the gain of a baseband circuit.

[Claim 6] A radio receiver as set forth in Claim 2 characterized by a variable gain block being divided into a variable gain block that changes continuously and a variable gain block that changes in steps, said variable gain block that changes in steps gain uniformly maintains the gain within one received slot and variable gain block that changes continuously changes the gain.

[Claim 7] A radio receiver as set forth in Claim 2 characterized by being equipped with a means that varies the gain of a high-

frequency amplifier and a high frequency converter in steps using control signals generated based on the received electric field strength measured by means of said received electric field strength measurement circuit.

[Claim 8] A radio receiver as set forth in Claim 7 characterized by preparing a few receiving modes in advance by means of combining the gain of each stage of said high-frequency amplifier, frequency converter, and baseband circuit and then selecting an optimal receiving mode from among said receiving modes based on values of the received electric field strength measured by means of a received electric field strength measurement circuit and setting the gain of each stage of the high-frequency amplifier, frequency converter, and baseband circuit.

[Claim 9] A radio receiver as set forth in Claim 7 or Claim 8 characterized by changing the gain setting of a receiver to be more exact based on values of the received electric field strength after the settings of the receiving mode in Claim 8 were set roughly.

[Claim 10] A radio receiver as set forth in Claim 7, Claim 8, or Claim 9 characterized by set the gain of a receiver up to the front of a requested receiving slot and uniformly maintaining the set gain while receiving a requested receiving slot.

[Claim 11] A radio receiver as set forth in Claim 7 characterized by initializing the gain setting of a receiver section to a receiving mode that can receive signals of electric field

strength defined in specifications when judging whether or not a receiving slot assigned to a station besides a local station of a TDMA system and then detecting the electric field strength of a receiving slot assigned to said station besides a local station.

[Claim 12] A radio receiver characterized by being equipped with a level detection device comprising a phase detector that detects phase quantities corresponding to demodulated signals of a demodulator that demodulates received signals which underwent frequency conversion to an intermediate frequency band or a baseband using a method determined in advance and a phase rotator rotates the phase of a demodulated signal of said demodulator based on the phase quantity detected by the phase detector, and then judges the received electric field strength of said received signals.

[Claim 13] A radio receiver characterized by being equipped with a gain control circuit that comprises a variable gain circuit that inputs analog signals, an A / D conversion circuit that converts the output of the variable gain circuit into a digital value, a detection circuit that detects an overflow state of the output of said A / D conversion circuit, and a control circuit that sets said variable gain circuit to a first gain quantity when said detection circuit detected an overflow state and also sets said variable gain circuit to a second gain quantity smaller than the first gain quantity when said detection circuit did not detect an overflow state.

[Detailed Description of the Invention]

[0001]

[Industrial Application] The present invention relates to a portable radio terminal used in radio communication systems and in particular to a small radio receiver that uses a direct conversion receiving system.

[0002]

[Description of the Prior Art] The demand for smaller and lower cost mobile terminals has increased following the development of mobile communications in recent years. The receiver for type of mobile terminal had especially serious problems of size and cost reduction of the radio section. There are two methods to achieve a reduced size of this receiving radio section. One method mounts micro-miniature circuit components at high densities and the other method uses a receiving system that does not require the use of large components. Since micro-miniature parts are generally more expensive than normal parts, the former does not lead to lower cost receivers. Therefore, when the cost is taken into consideration, the use of a receiving system that does not require the use of large components of the latter is more preferable. A direct conversion receiving system is one receiving system that can achieve this type of miniaturization and lower cost of the receiving radio section.

[0003] A direct conversion receiving system will be described below. A direct conversion receiving system is a receiving system that mixes received high frequency (RF) signals using a local

oscillator signal that has the same frequency as the RF signals, directly converts the frequency to baseband, and then detects the wave.

[0004] Fig. 29 shows an example of the composition of a conventional direct conversion receiver. After passing through an RF filter 202, the RF signals received from an antenna 201 are amplified by a high-frequency amplifier 203, divided into two channels, and then mixed with a sub carrier, that has the same frequency as the RF signals, from a local oscillator 206 in frequency converters 204, 207. This local oscillator is connected to the second frequency converter 207 through both the first frequency converter 204 and a 90° phase converter 205. The received RF signals are converted to baseband signals which have a phase relationship of 90° by means of the first and second frequency converters and are then amplified by baseband amplifiers 212, 213 after passing through low pass filters 210, 211. Thereafter, the wave is detected by means of a wave detection system used in ordinary quadrature detection such as a delayed wave detection (214).

[0005] Here, an A / D converter in the latter stage of the baseband amplifiers 212, 213 can be used when forming wave detection system into a digital system. In addition, AC couplings 208, 209 of the latter stage of the frequency converters prevent the amplifiers 212, 213 from saturating due to a DC (direct current) component produced by the frequency converters. Because of this, they are added

for the purpose of removing the DC component. In this example, although a 90° phase converter is added on the local oscillator side (reference carrier wave), adding it in the received signal path is also well known.

[0006] Because the direct conversion receiving system according to this composition directly converts the frequency of the RF signals to baseband and due to the fact that it does not have an intermediate frequency and an image response theoretically does not exist, it has attracted attention as a receiving system that can achieve even smaller sized receivers following the progress made in LSI in recent years due to factors such as not requiring steep-edged filters for removing images normally used in the RF stage of the super heterodyne system and the ability to allow filters for selecting baseband channels to undergo LSI integration.

[0007] Generally speaking, when moving a terminal in a mobile radio, received electric field strength will be changed along with the time in a so-called fading phenomenon. Since this fading produces deterioration of C/N and causes deterioration of telephone speech quality when demodulating received signals, it normally requires the envelope of the received signals to be made uniform using the automatic gain control (AGC) in the previous stage wave detection section. If the AGC operation in a direct conversion receiver is considered here, an operation must be performed that equivalently governs the amplitude fluctuations of the receiving envelope by means

of controlling the gain of the receiver section using gain blocks while fading or a digital signal process after an A / D converter.

[0008] Fig. 30 shows an AGC system that uses gain switching of a high-frequency amplifier described in Fig. 1 of document: "Performance of Direct Conversion Receiver with π/4-QPSK Modulated Signal" Proc. 41st IEEE Vehicular Technology Conference pp.822 to 828 (1991). In this system, after the received signals undergo quadrature demodulation (603,604) and amplification (609, 610), they undergo A / D conversion (611, 612), and signal level detection (613) and then the gain of the high-frequency amplifier (602) is controlled based on that information (614). Because this system can use an ordinary baseband delayed wave detection system as the wave detection (613) system, there are no problems of deterioration of the wave detection sensitivity in the static properties.

[0009] Although this is the case, when the AGC is drawn by the high-frequency amplifier only, the gain of the high-frequency amplifier will only be approximately 10 to 20 dB. Therefore, when there are significant variations in the fading, the dynamic range of the AGC will be insufficient resulting in a problem of not being able to obtain enough resistance to fading.

[0010] In contrast, in addition to the gain switching of a high-frequency amplifier (715), there is a system described in Fig. 1 of the document: "A New Incoherent Direct Conversion Receiver", Proc. 40st [sic] IEEE Vehicular Technology Conference pp. 668 to 674 (1990)

as well as a system (Fig. 31) that doubles the gain switching (714) using a baseband amplifier.

[0011] This system doubles the amplitude fluctuation by means of fading and switches the gain of a high-frequency amplifier and the gain of a baseband amplifier in steps (6 dB steps in the example of the previous document). And since the gain of the baseband amplifier itself is greater than the gain of the high-frequency amplifier, it is possible to obtain a dynamic range of an AGC amplifier other than the system in Fig. 32. Because the gain itself is controlled in 6 dB steps in this system, it is not possible to track a fading pitch (40 to60 Hz) when considering a vehicle speed in a system that uses, for example, a 900 MHz band radio wave. However, if there is a fading pitch of a walking speed (2 to 5 Hz), this system can sufficiently track the speed and be effectively used for cordless telephones or cellular telephones which can be held in one's hand and used.

[0012] This system has the problems listed below. As described above, since the gain block is small compared to a super heterodyne receiver in a direct conversion receiver, the flexibility of the fluctuation range of the gain that can be obtained in each block is smaller than a super heterodyne receiver. In other words, a design of a receiving radio section in a direct conversion receiver with very little flexibility is needed in order to ensure a dynamic range required for use as a mobile telecommunication device. Compared to this type of direct conversion receiver, the system of Fig. 31 can

ensure the dynamic range in the baseband stage to some extent since the gain of the baseband amplifier switches although, when, for example, the RF circuit itself is saturated with an incoming signals, the gain control in the baseband stage will be meaningless.

[0013] Namely, when an incoming signal is at a very high level, the gain control of only the high-frequency amplifier of the previous stage frequency converter will not be sufficient resulting in the possibility of the latter stage frequency converter circuit itself becoming saturated for this type of condition.

[0014] This is thought to occur when, for example, a cordless telephone or a cellular telephone is used very close to a radio base station. Furthermore, when using a cordless telephone at home, the cordless handset will momentarily receive a very large transmission power from the main telephone set when the cordless handset (= mobile terminal) is placed on the main telephone set (= base station). Saturation of this type of radio circuit must be prevented for this case.

[0015] If we consider when receiving a phase shift modulated signal in a conventional super heterodyne receiving system, the signals can be demodulated if the zero crossing point of the received signals in the intermediate frequency stage was saved even if the intermediate frequency amplifier is saturated. If the received signals are saturated at the baseband in a direct conversion

receiving system, the phase of the signals will not be saved making it impossible to demodulate the signals.

[0016] This was a problem of a direct conversion system and even though the gain of the high-frequency amplifier 702 was reduced as in the conventional method (Fig. 31) and the frequency conversion circuit 703 prevented from becoming saturated, there was a gain in the frequency conversion circuit 703 itself. Because of this, there was a problem of the latter stage baseband circuit becoming saturated.

[0017] Fig. 32 is the system shown in Fig. 2 of JP 61-236204A. This system receives the received signals by means of the antenna 401, performs high frequency amplification (402) and then frequency conversion (403, 404) on the signals. Thereafter, the system immediately performs A / D conversion (407, 408) and then all subsequent processing is handled by digital signal processing (412).

[0018] In order to ensure the dynamic ranges required by mobile receivers used for mobile communications and maintain a favorable receiving error rate in this method, a multi-bit A / D converter (for example, approximately 16 bits) must be provided. There is a problem of the power consumption of this type of multi-bit A / D converter and also the power consumption when using the subsequent digital signal processing becoming enormous. This is fatal as a receiving system of a mobile radio terminal that has limitations on the battery life.

[0019] Fig. 33 shows the composition described in JP 59-196629A "FM receiver" and is a method that provides resistance to fading by means of using a hard limiter for the direct conversion receiver.

[0020] Since the signals are demodulated by means of limiter discriminator detection, or namely, frequency detection in this method, there are problems of the frequency conversion being performed twice, more exact matching of the phase shift characteristics and the amplitude between the I and Q channels being required, and the hardware configuration becoming larger scale and more complex when compared to a normally used delayed wave detection method. Furthermore, there is another problem of the wave detection sensitivity in the static properties deteriorating by approximately 1 to 2 dB.

[0021]

[Problems to be Solved by the Invention] As described above, the gain control system used in a conventional direct conversion receiver had a problem of the dynamic range in the gain control system in the high-frequency amplifier being insufficient. In particular, although the dynamic range at the baseband stage could be ensured in a system that switches the gain of a baseband amplifier in steps, there was a problem of the baseband section becoming saturated due to an insufficient dynamic range of the RF section and the inability to sufficiently obtain a dynamic range of the entire radio device thereby making it impossible to receive signals.

[0022] In addition, there was another problem of the power consumption in a system that uses an A / D converter to digitally control the gain becoming enormous as well as another problem of the wave detection sensitivity in the static properties deteriorating in a system that uses a limiter to frequency conversion on the baseband signals after quadrature demodulation and convert the frequency to an intermediate frequency again.

[0023] Also, as described above, in order to apply a direct conversion receiver in an actual environment, there is a significant problem of providing a sufficient dynamic range from a practical point of view and achieving gain control of the receiver section that can withstand high-speed fading.

[0024] The present invention provides a radio receiver that can often obtain attenuation using a high-frequency amplifier with good accuracy when signals are input at high levels.

[0025]

[Means for Solving the Problems] In order to solve these types of problems in this radio receiver, a radio communication system that transmits high-frequency signals modulated by digital signals or analog signals wherein a radio receiver is provided with one or a plurality of high-frequency amplifiers for amplifying the high-frequency signals, a local oscillator that generates a reference signal at a frequency almost equal to the center frequency of the high-frequency signals, a phase shift means for acquiring first and

second reference signals whose phases intersect each other from the reference signal from the local oscillator, a first and a second frequency converter that multiplies the high-frequency signals and both first and second reference signals from the local oscillator and obtains a first and a second baseband signal, a first and second variable gain baseband circuit that that takes the signals output from the frequency converter as input signals and then provides a gain to the input signals, a demodulator for demodulating the output signals of the baseband circuit, and a received power measurement circuit that measures the electric field strength of received signals. This radio receiver is also characterized by being equipped with a function that varies the gain of at least one from among the high-frequency amplifier and the frequency converter, as well as a means that varies at least the gain of the baseband circuit and the gain of at least one from among the high-frequency amplifier and the frequency converter using control signals generated based on the received electric field strength measured by means of the received electric field strength measurement circuit.

[0026] This radio receiver is also characterized by being equipped with a means that varies the gain of a high-frequency amplifier and a high frequency converter in steps using control signals generated based on the received electric field strength measured by means of the received electric field strength measurement circuit.

[0027] A second invention is characterized by being equipped with a level detection device comprising a phase detector that detects phase quantities corresponding to demodulated signals of a demodulator that demodulates received signals which underwent frequency conversion to an intermediate frequency band or a baseband using a method determined in advance and a phase rotator rotates the phase of a demodulated signal of the demodulator based on the phase quantity detected by the phase detector, and then judges the received electric field strength of the received signals.

[0028] A third invention is characterized by being equipped with a gain control circuit that comprises a variable gain circuit that inputs analog signals, an A / D conversion circuit that converts the output of the variable gain circuit into a digital value, a detection circuit that detects an overflow state of the output of the A / D conversion circuit, and a control circuit that sets the variable gain circuit to a first gain quantity when the detection circuit detected an overflow state and also sets the variable gain circuit to a second gain quantity smaller than the first gain quantity when the detection circuit did not detect an overflow state.

[0029]

[Function] This radio receiver controls comparatively large amplitude fluctuations from among amplitude fluctuations of the received signals using gain switching of the high-frequency section and controls the amplitude fluctuations due to high-speed fading by

means of a continuous variable gain function of a baseband circuit. Because of this, the radio receiver has a function that allows comparatively high-speed fading to be tracked without placing a load on the circuit.

[0030] Also, since this radio receiver is equipped with a high-frequency amplifier and a variable gain block besides the baseband circuit in order to prevent the baseband circuit from becoming saturated, it is possible to provide a radio receiver with a wide dynamic range compared to a radio receiver that uses a conventional direct conversion receiving system.

[0031] The second invention is characterized by controlling the gain of the radio receiver by means of detecting the level of the received electric field strength using a rotational conversion. In particular, since the wave detection output component is equivalent to the received electric field strength and the decision circuit output is equivalent to the sin and cos components of the rotational quantity in a radio receiver that performs a baseband delayed wave detection, the level detector can be comprised by a small circuit compared with a conventional circuit.

[0032] The third invention monitors the output of the A / D converter of the receiver section and lowers only the gain of the variable gain circuit by only a first gain width if an overflow is detected. This invention also monitors the output of the A / D converter during only an observation time determined in advance and

when an overflow is not detected, compares a threshold value determined in advance with a maximum value within the observation time of the A / D converter and then estimates the received electric field strength. When this maximum is smaller than the threshold value, the control section of the gain control circuit will be controlled such that the gain of the variable gain circuit will be increased by only the second gain width smaller than the first gain width.

[0033]

[Embodiment] (First invention) In the following, the radio of the present invention is described using the drawings. Fig. 1 describes the basic composition of the radio receiver according to the present invention. The composition of the radio receiver in the present invention will be described using Fig. 1. The signals received from a receiving antenna 101 are supplied from a local oscillator 105 after they are given a gain by means of a high-frequency amplifier 104. The signals are then mixed with a reference signal at a frequency almost equal to the center frequency of the received signals by means of mixers 107, 108 and directly undergo frequency conversion to a baseband. A $\pi/2$ phase converter 106 is placed in the local oscillator output so as to make the two paths intersect with each other (IQ channel) after the frequency conversion. Placing this $\pi/2$ phase converter in the received signal path is also well known. After the received signals which underwent

frequency conversion to a baseband pass through channel filters 110, 111, they are amplified by means of baseband amplifiers 112, 113. This baseband amplifier only provides a degree of amplification obtains the most gain of the receiver section.

[0034] Received electric field strength detection (hereinafter, RSSI detection: Received Signal Strength Indicator) must be performed to baseband signals in this radio receiver. For this reason, an I channel (124) and a Q channel (125) of the output signal of the baseband amplifiers 112, 113 are sent to an RSSI detection circuit 115 (119). The RSSI detection circuit detects the received signal level and compares the detected received signal level to a reference voltage 116 and then feeds back that error signal to a radio circuit as a control signal. The control in the example of Fig. 1 is formed by three components, control 122 of the high-frequency amplifier (104), control 121 of the frequency converter (109), and control 120 of the baseband amplifier (114).

[0035] The reason why the frequency converter 109 has a variable gain function as in this example will be described next. The gain switching of the high-frequency circuit in a conventional direct conversion receiver was only performed by the high-frequency amplifier 702 as shown in Fig. 31. It is considered that the power supply of an RF amplifier will excessively turn OFF when a requested wave is at a very strong level. For this case however, the attenuation of the received signals is normally set to only about -40

dB. Therefore, even if the gain of only the high-frequency amplifier 702 was controlled, there was a possibility that the latter stage baseband filters 707, 708 and the baseband amplifiers 709, 710 might become saturated even more when the latter stage frequency converters 703, 704 had a conversion gain.

[0036] In contrast to this, since the radio receiver in the present invention has a function that controls the gain of a receiver at a minimum of three locations of a high-frequency amplifier, a frequency converter, and a baseband circuit, the radio section can be comprised to be resistant to receiving signals without saturating the baseband circuit even when the received electric field strength is very strong as in a conventional direct conversion receiver.

[0037] Furthermore, the RSSI detection method can also be performed by calculating the square root value of (I^2+Q^2) from an IQ signal as in a conventionally known method (for example, JP 4-24881B). In addition, although the received electric field strength is detected after the A / D (124, 125) converter in Fig. 1, it can also be detected in analog of course.

[0038] Even further, the high-frequency amplifier (104) in Fig. 1 can also be comprised with other stages. This is effective when assuming that it will be difficult for the high-frequency amplifier to have both low noise characteristics and a gain switching function when using the high-frequency amplifier 102 of the initial stage of the high frequency-amplifier block 104 as a low noise amplifier with

a fixed gain. For this case, the gain is controlled at a desired gain by means of the variable high-frequency amplifier 103 using the control signal 122 of the latter stage after the received signals are amplified by the low noise amplifier 102 of the initial stage. Although the high frequency-amplifier block 104 is not limited to two stages and can be any stage, the initial stage being equipped with a high-frequency amplifier with favorable noise characteristics is a characteristic of the radio receiver according to the present invention. In other words, placing a high-frequency amplifier that can switch gain in the initial stage is generally considered disadvantageous from the viewpoint of NF. Because of this, amplifying the received signals one time using a fixed gain high-frequency amplifier with a favorable NF as in the present invention will lead to improvements in the receiving sensitivity in the static properties.

[0039] Although the baseband amplifier 114 was considered as a variable gain element of a baseband circuit in this description, it is obvious that the variable gain element of the baseband in the radio receiver of the present invention can be either a baseband filter or a baseband amplifier.

[0040] In order to simply control the gain in the present invention, one or two or more attenuators can be placed in the previous stage or the latter stage of the high-frequency amplifier. In particular, even if input signals with strong level meet due to

the insertion of attenuators with multiple different attenuations, the gain in multiple stages can be controlled to the degree of the composition just by turning each attenuator ON and OFF.

[0041] A significant characteristic of the radio receiver of the present invention different from a conventional direct conversion receiver is the fact that a circuit besides the high frequency-amplifier 102 located before a baseband circuit controls the gain in order to prevent saturation of the baseband circuit 114 when there is a strong input. The gain is controlled by means of the frequency converter 109 as an example here.

[0042] Furthermore, the composition as shown in Fig. 2 can also be used. The signals received from a receiving antenna 301 are supplied from a local oscillator 306 after they are given a gain by means of a high-frequency amplifier 303. The signals are then mixed with a reference signal at a frequency almost equal to the center frequency of the received signals by means of mixers 304, 307 and directly undergo frequency conversion to a baseband. A $\pi/2$ phase converter 305 is placed in the local oscillator output in order to perform signal conversion such that the two signals intersect with each other (IQ channel) after the frequency conversion. After the received signals which underwent frequency conversion to a baseband pass through channel select filters 308, 309, they are amplified by means of baseband amplifiers 310, 311. After the output signals of the baseband amplifiers 310, 311 are converted to digital signals by

means of A / D converters 312, 313, they are sent to an RSSI detection circuit 314. The RSSI detection circuit detects the received signal level and compares the detected received signal level to a reference voltage 316 and then feeds back that error signal to a radio circuit as a control signal. In the example of Fig. 2, the control signal is fed back so as to control the baseband amplifiers 310, 311.

[0043] After directly converting the frequency of the received frequency to a baseband in this manner, a gain if given by means of a baseband AGC through a baseband filter that has a channel select and an anti-aliasing function after which A / D conversion and a route rolloff filtering wave detection is performed. The AGC control detects the received electric field strength using the baseband IQ signal after A / D conversion to find the difference between this signal and a reference level and then performed D/A conversion and controls the gain of the baseband amplifier after applying a loop filter.

[0044] Since the AGC signal of RSSI can be supplied to baseband amplifier using a digital signal in the composition shown in this figure, the frequency and the loop gain of the loop filter can be more accurately controlled compared to using an analog signal. In addition, control of the signal values as a control quantity can also be easily performed.

[0045] Fig. 3 describes an embodiment of a method that varies the gain of a frequency converter. In order to vary the gain of a frequency converter 1403, the gain of two frequency converters 1401, 1402 (dual system) can be independently controlled although there is a possibility that independent control might be difficult due to an amplitude offset error that occurs between two frequency converters. For this type of circumstance, another method has also been considered that varies the gain of the high-frequency frequency conversion by means of changing the injection level of the local oscillator. As shown in Fig. 3(a), this method varies the gain of the amplifier of a local oscillator 1405 output stage that supplies a reference carrier signal to the dual system frequency converter 1403, using a control signal 1408 from a gain control circuit 1409. Compared to when the frequency converters 1401, 1402 are independently controlled, because this method uses one control line and a control signal 1408 is common to the frequency converters 1401, 1402, fluctuations on gain between the two frequency converters is reduced.

[0046] Fig. 3 (b) showed the relationship between the local oscillator injection level and the gain of the frequency converter. Here, if the injection level of the local oscillator is excessively large, the gain of the frequency converter will be saturated. However, if the gain of the (section 1406) frequency converter is used at the section (section 1407) that is linear with respect to the

local oscillator input level, a favorable gain control will be possible. In this example the gain of the frequency converter can be varied between 10 dB to 20 dB by means of controlling the injection level of the local oscillator between -20 dBm to -10 dBm.

[0047] Another embodiment of the radio receiver according to the present invention will be described. The radio receiver of the present invention changes the gain of the high-frequency amplifier 104 and the frequency converter 107 in steps "roughly" and also changes the gain of the baseband amplifier 114 continuously. If changed in this manner, the gain of the entire receiver can be apparently changed continuously. Therefore, the radio receiver of the present invention provides a characteristic that continuously changes the gain of a baseband amplifier without changing it in steps compared to the composition of Fig. 20 according to a conventional invention and also has an advantage of the ability to be even more effectively used during high-speed fading.

[0048] Another example of the radio receiver according to the present invention will be described. The radio receiver of the present invention is equipped with a means that varies the gain of the high-frequency amplifier and the frequency converter in steps and also continuously varies the gain of the baseband circuit using control signals generated based on the received electric field strength measured by means of a received power measurement circuit. In addition, the radio receiver according to the present invention

adjusts the gain of a dual system baseband circuit. Even though this is the case, approximately 80 dB is required for the gain of the baseband amplifiers 112, 113 in the composition of Fig. 1. The gain will become very large in this manner making it difficult to spread the gain of the two baseband amplifiers 112, 113 (whose gain is continuously varied) over a wide dynamic range.

[0049] Thereupon, the radio receiver according to the present invention is characterized by having a composition that realizes the gain of the baseband amplifiers 112, 113 using two blocks to suppress the gain of the baseband amplifier whose gain is continuously varied to approximately 40 dB and compensate for that the insufficient portion using an amplifier that discretely switches the gain of the baseband amplifier of the previous stage. The advantages when discretely switching the gain of an amplifier are improved accuracy of the gain compared to when the gain is continuously varied and also simplified circuitry. In addition, the effect of suppressing the gain of the baseband amplifiers (112, 113) whose gain is continuously varied is that any unbalance between the two amplifiers of the gain (between the I channel and Q channel) is also suppressed. The baseband filters 110, 111 or the frequency converters 107, 108 can also have the function of an amplifier that discretely switches the gain of the baseband amplifier of the previous stage. Another baseband circuit can also be separately provided in the previous stage of the baseband circuit 114.

[0050] Although the embodiments above described when the gain of a baseband circuit was continuously varied, another embodiment shown below will describe when the gain of the circuit of a receiver section is discretely varied. This can be applied when there is favorable resistance to comparatively low-speed fading or namely, when using a cellular telephone while walking. For this case, there is no need to use an AGC amplifier whose gain is continuously varied. This also has exceptional points of even better circuit feasibility and more simplified circuit configurations thereby making it possible to use a variable gain amplifier whose gain is discretely varied.

[0051] Fig. 4 and Fig. 5 will be used to describe this. Both Fig. 4 and Fig. 5 are frames of a TDMA or a TDD system. Fig. 4 shows when a receiving level change 1701 is at a high speed and Fig. 5 shows when a receiving level change 1801 is at a low speed. 1705 and 1805 represent one frame length and 1702 and 1802 represent one slot length.

[0052] Here, if RX1 is a requested receiving slot in Fig. 4, a fading notch will be set into the requested receiving slot RX1 (1703, 1704) and an AGC amplifier whose gain is continuously varied will be required in order to prevent this resulting effect. In contrast to this, when the change speed of the receiving level is slow as shown in Fig. 5, there is a slight change in the received electric field strength between the preceding frame RX1 (1803) and the next frame RX1 (1804). Therefore, when there is almost no change in the radio

wave environment between multiple slots as shown in Fig. 5, the gain of the radio receiver section (gain of the amplifier and the frequency converter) between the receiving slots of certain frames can be kept constant during a receiving operation. Because of this, the gain of the receiver section when a preceding frame (1803) is received is held in the memory and this value can also be used without any changes as an initial value when receiving the requested receiving slot (1804) of a next frame.

[0053] The radio receiver according to the present invention is also characterized by preparing several receiving modes using combinations of the gain of each circuit while receiving in order to simplify the radio section gain settings while receiving (gain settings of the amplifier and the frequency converter) even more and is further characterized by selecting an optimal receiving mode from among these receiving modes based on the value of the received electric field strength and then setting the gain of each stage.

[0054] In the following, an embodiment of the present invention will be described in detail using drawings and flow charts. In this description, three devices; a high-frequency amplifier, a frequency converter, and a baseband amplifier are considered as a variable gain block as shown in Fig. 1.

[0055] Table 1 shows one example of the receiving mode settings in this radio receiver.

[0056]

[Table 1]

Receiving mode	Antenna terminal input level (dBμ)	Gain of each stage (dB)		
		High-frequency amplifier	Frequency converter	Baseband amplifier
Mode 1	0-20	20	20	60
Mode 2	20-40	20	20	40
Mode 3	40-60	20	0	40
Mode 4	60-80	20	0	20
Mode 5	80-100	0	0	20

Table 1 shows five modes obtained using the values of the received input levels at an antenna terminal. Two types of gain 0 dB or 20 dB can be set for the high-frequency amplifier, two types of gain 0 dB or 20 dB can be set for the frequency converter, and three types of gain 20 dB, 40 dB, and 60 dB can be set for the baseband amplifier. As an example here, receiving mode 1 is a receiving mode in which the received input level at an antenna terminal is set when the levels are 0 dBμ to 20 dBμ. This mode 1 is a mode that is set when the input signal level is the weakest or namely, when receiving signals at a receiving sensitivity level and the gain of that portion and each circuit in the receiver section is becoming higher. Here, the gain of the high-frequency amplifier is 20 dB, the gain of the frequency converter is 20 dB, and the gain of the baseband amplifier is 60 dB. If the input signal increases 20 dB, the mode will move to mode 2 and the gain of the baseband amplifier will decrease 20 dB and be set to 40 dB. In addition, although the mode will move to mode 3 if the input level increases 20 dB, this embodiment is characterized by the

gain of the frequency converter decreasing 20 dB without the gain of the baseband amplifier decreasing 20 dB in order to prevent saturation of the baseband amplifier. In the same manner, the gain of the high-frequency amplifier is decreased in order to prevent saturation of the frequency converter in mode 5. In other words, the circuit of the previous stage controls the gain in order to prevent signals from being transferred which would saturate the latter stage circuit.

[0057] Fig. 6 is an example of a level diagram when using this receiving mode to amplify received signals. A receiver input level 2006 received with an antenna 2001 is amplified by means of a high-frequency amplifier 2002, a frequency converter 2003, and a baseband amplifier 2004. In this figure, 2007, 2008, and 2009 are the gain portions of the high-frequency amplifier, the frequency converter, and the baseband amplifier, respectively. The signals at the baseband amplifier output are amplified up to the level of 2010 and then transferred to an A / D converter 2005.

[0058] The mode switching system described above is especially effective when this radio receiver is used in a TDMA or a TDD system. Fig. 7 shows the frame structure in a TDMA or a TDD system. In Fig. 7, 1501 is one frame length and RX1 or RX2 are receiving slots. When RX1 is a requested receiving slot and will receive 1508, the receiving mode will be set up to just before the slot 1507 receives a signal based on the received electric field strength detected at the

RX1 receiving slot (1502) in one previous frame. In other words, the receiver section gain is set for the slots 1503 and 1508 at equal receiving levels. This is based on the fact that the value of the received electric field strength at the preceding frame RX1 (1503) and at the succeeding frame RX1 (1508) is regarded to be almost equal if the fading speed is sufficiently slow compared to one frame length (1501). Even further, since the receiving level between the one slot 1508 is regarded to have not changed, the mode that was set is fixed while slot 1508 receives signals.

[0059] Next, the method to detect the received electric field strength and the method to find the received electric field strength at an antenna input terminal from the signal output level of a baseband amplifier in the radio receiver according to the present invention will be described in detail using Fig. 8.

[0060] Knowing the absolute value of the received electric field strength at an antenna input terminal in a receiver is necessary in order to prevent saturation of the high-frequency amplifier (104 in Fig. 1) and the frequency converter 109 during a high-level input. The reason it is easy to measure the level of signals which were received by this receiver is the output point of baseband amplifier (802). Thereupon, this radio receiver has a characteristic of calculating the value of the received electric field strength at the antenna input terminal of a receiver using the absolute value of RSSI (PBB) at the baseband amplifier output, the gain (R) of the high-

frequency amplifier 104, the gain (M) of a frequency converter (109), and the gain (B) of the gain (114) of the baseband section. This can subtract the gain of the baseband amplifier, the gain of the frequency converter, and the gain of the high-frequency amplifier from the value of RSSI (output level of baseband amplifier) detected at the baseband amplifier output (803). The gain of these circuits is sequentially updated for every receiving slot and stored in the memory each time.

[0061] Next, one procedure of a method to initially set a receiving mode after turning ON the power supply of a radio receiver will be described using Fig. 9. The problem when initializing the gain of a receiver is the fact that there is absolutely no information concerning the signal level to be received. Because of this, when the signal level is extremely large or extremely small, the received electric field strength cannot be measured resulting in a problem of not being able to set the gain of the receiver.

[0062] The radio receiver in the present invention set attempts to measure the received electric field strength (904) while sequentially setting the receiving modes (903, 907) and then sets the optimal receiving mode that receives the incoming signal level (906) when the detection of the received electric field strength becomes an allowable C/N (C: received signals, N: receiver thermal noise) (905). The procedure to sequentially set this receiving mode (907) should be sequentially set from receiving modes with a slight gain. The reason

for this is to avoid saturation of the A / D converters (124, 125) when there is an excessive input. In other words, the receiving mode will be set when the gain of the receiver section is set in order of mode 5 -> mode 1 and the received electric field strength can be measured in the example of Table 1. When it is preferable to reduce the time required to sequentially set the receiving mode here, a method that searches every other mode (other than modes 4, 2 as in modes 5, 3, 1 in the example of Table 1) is effective. This method is also effective when measuring the received electric field strength of other slots besides the requested receiving slot.

[0063] The reason why the received electric field strength of other slots is measured is to understand the operating condition of other channels from a normal condition or a so-called empty channel search in order to allow movement to other slots when the slot being used receives interference. Fig. 10 shows an example of this action. This measures the received electric field strength of slots (in this example 2202) besides the requested slots (2201, 2203) of a TDMA communication. For this case, the received electric field strength of the other slots is completely unknown. Therefore, there is a possibility that the radio section may become saturated depending on the settings of the gain of the radio receiver section. For this reason, a method that at first roughly sets the gain as in this case is effective from the viewpoint of shortening the required time of the received electric field strength.

[0064] Next, the determination method of a receiving mode during ordinary reception will be described using Fig. 11. Here, we will consider when RX1 of Fig. 7 is being received. The received electric field strength P is measured (1105) at RX1 (1503) after the power supply turns ON (1102) and the above-mentioned initial settings (1103) are made. If the fading pitch is sufficiently long compared to one frame length (1501), 1503 and 1508 of Fig. 7 will be thought to have almost equal receiving levels. Because of this, a receiving mode is determined (1106) to receive the electric field strength (= received electric field strength of 1508) measured at 1503 and the slot (1508) of the next frame (1107) is received (1108).

[0065] The method above set the receiving gain based on the received electric field strength measured at slot 1503 when receiving slot 1508 from among the reception frames shown in Fig. 7. Although this is the case, the gain of the receiver section when actually receiving slot 1508 is preferably set using the received electric field strength of slot 1508 itself.

[0066] This method will be described below. Fig. 12 shows an example of the slot configuration of a TDMA or a TDD system. In this figure, 1601 is a requested receiving slot, 1602, 1603 are adjoining receiving slots, and 1604, 1605 are guard times. Slot 1601 is comprised by a start symbol 1606, a preamble 1607, an identification word 1608, and an information signal 1609. As an example, if the received electric field strength can be measured at the preamble 1607

interval, the receiving mode and the gain can be set in order to receive the information signal 1609 portion of this slot based on that information.

[0067] The procedure of this method will be described using Fig. 13. n = 1 noted in 1304 in Fig. 13 shows that at present, the requested receiving slot is already being received. The gain settings of the receiver section at this time depend on the receiving mode that was set in the initial setting 1303. In 1305, the received electric field strength P' of a desired wave in the slot currently receiving the signals is measured using the top section (for example, preamble 1607 of Fig. 12) of the receiving slot and then the receiving mode is set based on this value (1306) and the signals received (1307). The initial value of the receiving mode set in the received electric field strength measurement (1305) from the next frame (n = 2) can be set to the receiving mode used when receiving one previous frame (n = 1). For example, when signals are received using mode 3 at n = 1, mode 3 can be used as an initial value when measuring the received electric field strength (1305) at n = 2. In addition to this, if the intention is to avoid saturation of the A / D converters (124, 125 of Fig. 1) when measuring the received electric field strength (1305) at n = 2, mode 4 with a slight grade 1 gain can be used as the initial value when measuring the received electric field strength (1305) at n = 2.

[0068] When the variable gain width of the receiver section is too large (20 dB in Table 1) and the gain setting is too rough during the receiving operation according to the receiving modes described above, the variable gain width can be narrowed such as being set to 5 dB. If this value is made excessively small, the number of receiving modes will increase and problems such as time being required to initialize the settings and the control becoming complicated will occur. In order to solve these problems, the radio receiver in the present invention is characterized by finely setting the gain of the receiver based on the value of the received electric field strength after roughly setting the gain of the receiver using the settings of the receiving mode.

[0069] This method will be described using Fig. 14 and Fig. 15. Measuring the received electric field strength P of 1503 and then setting the receiving mode based on this value in order to receive 1508 of Fig. 7 will be considered. Fig. 14 is a receiving level diagram of a receiving mode that was set up in order to measure the electric field strength P at 1503 and receive 1508. In Fig. 14, the level diagram (2108) indicated by the solid line shows when the receiving mode 1 of Table 1 is set. The gain of the high-frequency amplifier (2102), the frequency converter (2103), and the baseband amplifier (2104) is 20 dB, 20 dB, and 60 dB, respectively.

[0070] Here, the output level (2106) of the baseband amplifier (2104) must be within a range (2110) between the saturation level

(2111) of the A / D converter (2105) and the minimum input level (2112) required to maintain the bit accuracy of the A / D converter. Furthermore, if the amount of fluctuation between the electric field strength P detected at the slot 1503 of Fig. 7 and the electric field strength actually received at the slot 1508 is taken into consideration, it is preferable for the gain of the receiver section that was set in order to receive the slot 1508 to see a margin of that amount of fluctuation and the output level (2106) of the baseband amplifier to be set so as to reach the exact center of the input range 2110 of the A / D converter. If set in this manner, when the input range 2110 of the A / D converter is 20 dB, the difference between the received electric field strength P at the slot 1503 and the received electric field strength at the slot 1508 can correspond to up to 10 dB.

[0071] Fig. 15 shows the setting procedure of this method. This procedure uses a mode that was set based on the received electric field strength P measured at slot 1503 to calculate the baseband amplifier output PBB when the received electric field strength P is received and judge whether this value is higher or lower than the center (or a certain reference level) of the input range of an A / D converter (1002). If this value is higher, the gain of the baseband amplifier will drop (1003) by a core width (for example, 5 dB) smaller than the minimum width of the gain of the baseband amplifier that can be set (20 dB in this example) that is set to the receiving

mode in Table 1. Conversely, when PBB is lower than the center (or a certain reference level) of the input range of an A / D converter, the gain of the baseband amplifier will rise by a small core width (for example, 5 dB) (1004).

[0072] Fig. 16 shows a flow chart of this method. In this example, the next frame will be received after finely adjusting the gain (1211) shown in the flow chart of Fig. 15 in the receiving mode (1206) that was determined based on the value of the measured received electric field strength P (1205). 2107 of Fig. 14 shows a receiver section level diagram that follows the receiver section gain set at this time. This finely adjusts the gain of the receiver section until the baseband amplifier output 2106 when using the gain set by the receiving mode reaches the value shown in 2107.

[0073] This method has an advantage of being able to achieve a radio receiver that can more flexibly correspond to changes in the received electric field strength compared to when using a receiving mode only in order to finely adjust the gain after selecting a receiving mode. Inserting this method at 909 of Fig. 9, 1111 of Fig. 12, and 1311 of Fig. 13 allows it to be effectively used as a process after setting a receiving mode.

[0074] Although the method to measure the received electric field strength of an empty channel was already described, an exact value of the received electric field strength is not required if it is possible to only judge whether the value is higher or lower than a

certain value. Setting the receiving mode for this type case will be described. The radio receiver according to the present invention is characterized by setting the initial gain of the receiver section to a receiving mode in the state that allows "the signal of the electric field strength defined in the specifications" to be received during an empty channel. Here, the "electric field strength defined in the specifications" is a value generally defined in the specifications of a system such that if the received signals are equal to or more than this electric field strength, the channel state will be "currently being used" and if the received signals are equal to or less than this electric field strength, the channel state will be "not being used." Therefore, if the A / D converter becomes saturated when setting the gain of this radio receiver and the gain of the receiver section is too large while searching for an empty channel, the state of the measured slot can be immediately judged to be "currently being used" and if not saturated, can be immediately judged to be "not being used."

[0075] In this description, although three devices; a high-frequency amplifier, a frequency converter, and a baseband amplifier are considered as the variable gain block as shown in Fig. 1, the present invention is not restricted to this composition only.

[0076] Next, another embodiment of the present invention will be described using Fig. 17. In Fig. 17, the IQ output signals from two (dual system) frequency converter (2301, 2302) and baseband filters

(2303, 2304) is switched by means of a switch (2305) that performs a switch using a clock signal from an oscillator (2310) and then the IQ output signals are alternately input into a baseband amplifier (2308) at the clock period. The baseband amplifier (2308) is an ACG [sic] amplifier in which the gain is controlled by control signals (2311) from a digital signal processing section (2315). After gain is applied to the incoming signals by means of this amplifier, they undergo A / D conversion (2309) and are input into a digital signal processing section (2315) by means of the switch (2305) synchronized with a switch (2312) on the input side. The I/O switch here is set to be an input side switch when located at the 2305 side, an output side switch when located at the 2313 side, an input side switch when located at the 2307 side, and an output side switch when located at the 2314 side.

[0077] According to this composition, there are advantages of simplified circuitry and lower power consumption because the baseband AGC amplifier (2308) and A / D converter (2309) which required a conventional dual system could be achieved with a single system. This composition also has an effect of being able to solve the conventional problem of unbalance of the gain and amplitude between channels of an IQ2 system due to incomplete circuits.

[0078] To sum up the description above, since the present invention can control comparatively large amplitude fluctuations from among the amplitude fluctuations of the received signals by means of

gain switching of a high-frequency section and also control amplitude fluctuations due to high-speed fading using a continuous variable gain function of a baseband circuit, this invention has an effect of allowing comparatively high-speed fading to be tracked without placing a load on the circuit. In addition, since this invention is equipped with a means that varies the gain of the high-frequency amplifier and the frequency converter in steps and also continuously varies the gain of the baseband circuit, it also has an effect of suppressing unbalance of the gain between an I channel and a Q channel compared to when using a variable gain amplifier that continuously varies a comparatively large gain.

[0079] Even further, since the radio receiver in the present invention has a function that controls the gain of the receiver at a minimum of three locations of the high-frequency amplifier, the frequency converter, and the baseband circuit, the invention has an effect of allowing the radio receiver to have a composition with a wide dynamic range that is resistant to receiving without saturating the baseband circuit even when the received electric field strength is very large compared to a conventional direct conversion receiver.

[0080] Even further, since the radio receiver according to the present invention is provided with a means that prepares several receiving modes using combinations of the gain of each circuit while receiving in order to simplify the radio section gain settings while receiving (gain settings of the amplifier and the frequency

converter) even more by selecting an optimal receiving mode from among these receiving modes based on the value of the received electric field strength and then sets the gain of each stage, the invention has an effect of being able to set the gain of a high-speed receiver section gain compared to a conventional receiver.

(Second invention) As described above, since the received electric field strength will be changed along with the time when moving a communication terminal, the received electric field strength must be detected and the amplification factor and attenuation factor must be adjusted to obtain a suitable signal amplification. A general method to detect the electric field strength of the received signals in a base band range was one that alternately detected the squared sum of the baseband signal of two channels (Ich, Qch) as shown in Fig. 18.

[0081] However, since the baseband signals of Ich, Qch are both multi-bit digital signals, they must be multiplied by multipliers 3401, 3402 of multi-bit digital signals and then undergo a summing process using a digital adder 3403. Consequently, there were problems of these digital multipliers and adders having large circuit structures and significant power consumption.

[0082] Thereupon, the invention of a level detection circuit of received signals that can be comprised with substantially less digital circuits, such as a digital multiplier, will be described.

[0083] Fig. 19 shows a basic example of the composition of the radio communication device of the present invention. The radio frequency (RF) signals received from the antenna undergo frequency conversion to a base band range by means of a radio receiver section of 3001. The radio receiver section 3001 can be applied here regardless of the specific receiving system such as a direct conversion receiving system or a super heterodyne receiving system.

[0084] The baseband signals which underwent frequency conversion are converted to digital signals by means of AD converters 3002, 3003. This digital baseband signal is input into a wave detector 3004 and then a phase signal relative to the reference wave generated by the wave detector 3004 is reproduced. This relative phase signal is input into a decision circuit 3005 and converted to signals such as digital sound or data.

[0085] Simultaneous with this, the reproduced relative phase signal is input into a phase detection circuit of 3006 and a phase quantity [Φ] is output based on the coordinate axis within a complex plane from the relative phase information that was detected. A level detection circuit of 3007 inputs the phase quantity [Φ] at the 3006 output and the wave detector output signal of 3004 and then converts the wave detector output of 3004 onto a coordinate axis by means of rotating within a complex plane by only the phase quantity [Φ] found in 3006.

[0086] When a level detector is comprised in this manner, the in-phase component of the wave detector output that was converted onto a coordinate axis will be equivalent to the baseband signal level. Because of this, an even simpler composition compared to a conventional device can be achieved and the electric field strength of the received signals can be detected by means of detecting the magnitude of the in-phase component of the wave detector output.

[0087] Next, another example of the composition of the radio communication device of the present invention will be described referring to Fig. 20. The function of the phase detection means 3006 in Fig. 19 can also be comprised using the wave detector 3004 and an example of the composition for this case will be described below. Fig. 20 uses symbols identical to the composition elements of Fig. 19 and the description of these composition elements will be omitted here. In addition, although the case described here is when a $\pi/4$ shift QPSK signal is used as an input signal and baseband delayed wave detection is used for the detection system, the present invention is not limited to input signals or a wave detection system.

[0088] In Fig. 20, the output signal of the wave detector 3004 is sampled by sampling circuits 3011, 3012 using a clock frequency of a symbol rate determined in advance. This sampling circuit removes level components the signal itself has from the output signal that underwent delayed wave detection. For example, as shown in Fig. 26, the resurge signal of the output signal of the wave detector 3004

forms a locus such as a broken lines in response to the transition of the symbols. If this is sampled at an optimum timing, representative points shown by dark points can be found. The distance from the origin point of this sampling signal is equivalent to the receiving level of the baseband signal. Therefore, the present invention detects the received electric field strength by means of finding the distance from the origin point of the wave detection output signal by rotational conversion of the wave detection output signal for this received electric field strength.

[0089] The output signal of this sampling circuit is input into a phase detection circuit of 3013. In this phase detection circuit, the phase Φ is output from the output signals of the sampling circuits 3011, 3012 based on the coordinate axis Ich shown in Fig. 21. For example, in Fig. 21, when there are 3200 input points, $\Phi = -\pi/4$ will be output. In the same manner, when there are 3201 input points, $\Phi = \pi/4$ will be output, when there are 3202 input points, $\Phi = -3\pi/4$ will be output, and when there are 3203 input points, $\Phi = 3\pi/4$ will be output. Thereupon, the in-phase component will be output after the rotational conversion of the rotational conversion section 3014 of Fig. 20 inputs the sampling circuit output of the sampling signals 3011, 3012 and the Φ (phase detection circuit output of the phase detection circuit 3013) and the wave detector output, sampled at the symbol rate, has undergone rotational conversion using only the detected phase.

[0090] Next, the ability to detect the input signal level in the baseband by means of phase rotating the wave detector output will be described in light of the example. Fig. 22 shows a block diagram of a baseband delay wave detector. Baseband delayed wave detection is a system that uses an output signal from A / D converters 3101, 3102 and a reference wave that is a signal delayed by delay devices 3103, 3104 one symbol time to detect waves by means of performing complex multiplication of these signals using a multiplier section 3105. This system uses an adder 3106 to find the in-phase component Idef (n) of the output signal and also uses a subtractor 3107 to find the quadrature component Qdef (n) of the output signal. Here, Idef (n) and Qdef (n) are both expressed by the following equations.

[0091]

$$Idef(n) = I(n)*I(n-Ts)+Q(n)*Q(n-Ts)$$
$$Qdef(n) = Q(n)*I(n-Ts)-I(n)*Q(n-Ts)$$

Here, Idef and Qdef are delayed wave detection output values, I (k) and Q (k) are digital baseband signals at sampling time ts = k, and Ts is one symbol time. In contrast, the distance from the origin point of this delayed wave detection output signal is r (n), then the following equation will be true.

$$r(n)2 = (Idef(n))2 + (Qdef(n))2$$
$$= (I(n)*I(n-Ts))2 + (Q(n)*Q(n-Ts))2$$
$$+ (Q(n)*I(n-Ts))2 - (I(n)*Q(n-Ts))2 \quad \cdots(1)$$

The object of the present invention is to detect the received signal level by means of fading that generates when a radio receiver moves.

Normally, the fading pitch determined by the movement speed of the radio receiver can be assumed to be sufficiently long with respect to one symbol interval that is determined by the transmission speed. Although level fluctuations contained in the signal itself are contained in a π/4 shift QPSK signal, the output sampled at a symbol rate timing does not contain this level fluctuation component as shown in Fig. 21. Therefore, it is thought that there are almost no level fluctuations due to fading in a one symbol section close to this sampling point. And because of this, approximately

$$I(n-Ts)\,2 = I(n)2 \;,\; Q(n-Ts)\,2 = Q(n)2$$

can be replaced in equation (1) and the third and fourth lines of Equation 1 eliminated to result in the following equation.

$$r(n) = I(n-Ts)I(n) + Q(n-Ts)Q(n)$$
$$= I(n)2 + Q(n)2 \quad \cdots(2)$$

The right side of Equation (2) is the signal power of the baseband signal I(n) + jQ (n). As stated above, the distance r (n) from the origin point of the output signal during the baseband delayed wave detection is equivalent to the power of the baseband signal. Therefore, the electric field strength of a received wave can be found by finding the distance from the origin point of a detected wave output signal.

[0092] The present invention can be used as part of an AGC circuit within a receiver. This is particularly effective in a direct

conversion receiver that must detect the level fluctuations of the received signals at baseband.

[0093] The principle when applying the present invention to an AGC circuit will be described below. Generally speaking, the received signals can be expressed by the level fluctuation components the signal itself has and the sum of the level fluctuation components due to fading. The AGC circuit compensates for the level fluctuation components due to this fading. The level fluctuation speed due to fading is slow enough with respect to the level fluctuation speed which the signal itself has. Therefore, the AGC had to either remove the level fluctuation components of the previously received signals using a conventional LPF or absorb the fluctuation components of the received signal level by means of averaging on the baseband.

[0094] Although this is the case, since there are no fluctuation components the signal itself has at the focus point (point sampled at the symbol rate) of a wave detector output signal in an ordinary phase modulation system such as PSK or DPSK, if this focus point is input into a level detection circuit, an LPF or an averaging circuit which were conventionally required will not be needed thereby making it possible to realize comparatively small circuits.

[0095] Fig. 23 shows a compositional example when employing the present invention in a baseband AGC system. The output signals of baseband amplifiers 3301, 3302 are converted to digital signals by A / D converters 3303, 3304. Then, phase signals are reproduced by a

wave detector 3305 based on the digital baseband signals and converted to data signals by a decision circuit 3308. In contrast, the output signals of the wave detector are sampled by sampling circuits 3306, 3307 and the receiving level detected by means of a level detection circuit 3309 as described above.

[0096] As an example here, the signal Idef (Ts) + jQdef (Ts) sampled at highest point of the noise margin of the eye pattern that underwent delayed wave detection converges at four types of signal points on a complex plane as shown in Fig. 21. If the distance from the origin point of each of the four points is r (Ts) at this time then r (Ts) will be equivalent to the power of the received signals according to Equation (2). When an ideal delayed wave detection is performed, r (Ts) will be mutually equal to the four types of signal points. Therefore, after the output of the delayed wave detection sampled at the symbol rate is rotated on one of the coordinate axes for each of the symbols, the received signal power can be calculated by finding the in-phase component. For example, performing a rotation operation on coordinate axis Ich in Fig. 21, the received signal power will be expressed by the following equation.

$$r(Ts) = I\,def(Ts) \cdot \cos\Phi + Qdef(Ts) \cdot \sin\Phi \quad \cdots(3)$$

Since Φ is either the mapping mode shown in Fig. 26 or $\pm \pi/4$, $\pm 3\pi/4$ here, cos Φ and sin Φ which correspond to this will be values from among $\pm 1/(2^{1/2})$. If the decision circuit output is a value

represented by (i, q) of Fig. 21, cos Φ and sin Φ of Equation (3) can be expressed by a value $1/(2^{1/2})$ times the decision circuit output.

[0097] In other words, as an example of the circuit composition of the present invention, a circuit composition can be achieved such as level detection circuit 3309 of Fig. 23 by considering the decision circuit output and the delayed wave detection output as inputs. Even though the function of this level detection circuit 3309 is a rotational conversion function, the circuit can be realized using inverter circuit 3309-a, exclusive OR (EXOR) circuit 3309-b, and adder circuit 3309-c and compared to the conventional circuit shown in Fig. 18, the circuit can be substantially miniaturized.

[0098] When the above-mentioned decision circuit 3308 detects a signed bit of the delayed wave detection output, the level detection circuit of the present invention can also perform the detection using the delayed wave detection circuit output only without inputting the decision circuit output in this compositional example. Fig. 24 shows an example of the composition of the level detection circuit for this case. The I and Qch signals are converted into digital signals by the A / D converters 3501, 3502 and the signals judged by the decision circuit 3504 after delayed waves are detected by the delayed wave detection circuit 3503. In addition, after the output from the delayed wave detection circuit 3503 is sampled at the symbol rate by the sampling circuits 3505, 3506, the MSB of the digital value will be detected (3507, 3508) and then the absolute value detecting

circuits 3509, 3510 will find the absolute values of the digital values of both I and Qch. After the adder circuit 3511 adds these two absolute values, constant multiplication of 1/#2 will be performed by the counter circuit 3512 for this case. This operation makes it possible to detect the receiving level. Even further, the effect of detecting the baseband level using a comparatively simple circuit composition with the output of the wave detector considered as the input as described above is not restricted to combinations of π/4 shift QPSK baseband delayed wave detection but can also be applied to radio receivers which widely use a phase modulation system. For example, the same effect can be expected when using a QPSK modulation system - synchronous detection system.

[0099] When using the present invention as part of an AGC circuit, finding the absolute value of the received power is not always necessary and understanding only the difference of the detected receiving level from a reference value is sufficient. For example, the level relative to this reference value can be detected by the difference circuit 3310 and considered to be the input of the integration circuit 3311 in the example shown in Fig. 23. A negative feedback AGC circuit can be formed by means of using the converter 3312 to convert the output of the integration circuit 3311 into an amplitude control value of a baseband signal and then controlling the gain of the baseband amplifiers 3301, 3302. If, for example, the baseband amplifier is a digital control system and the converter of

3312 is a ROM table that converts the integration circuit output into a digital control signal or a voltage control system, it is possible for them to be comprised by a DA converter and an LPF.

[0100] As described above, the radio receiver that uses a level detection circuit is characterized by detecting the receiving level using a rotating map. In particular, since the wave detection output signal is equivalent to the received electric field strength and the decision circuit output is equivalent to the sin and cos components of the amount of rotation in a radio receiver performs baseband delayed wave detection, a small circuit structure can be realized compared to a conventional circuit. Moreover, when an AGC device using a level detection circuit is formed, high-speed variable gain control can be performed without losing the dynamic range of the receiver section when rapid fluctuations occur in the input amplitude.

(Third invention) An embodiment of the radio receiver using the AGC system of the present invention will be described in detail below referring to the drawings.

[0101] Fig. 25 is a block diagram showing one embodiment of the present invention. After the received signals received by the antenna section 4001 pass through the high-frequency section 4004, a quadrature demodulation section 4009 performs frequency conversion on two baseband signals, an in-phase component (hereinafter, Ich) and a quadrature component (hereinafter, Qch). The quadrature demodulation

section 4009 is comprised by a local oscillator 4005 and a mixer that multiplies the output of the local oscillator and the received signals. The received signals, which were converted into a base band, are filtered by means of low-pass filters 4010, 4011 and are then amplified by a variable gain amplifier 4014 and converted into digital signals by an analog / digital converter (hereinafter, A / D converter). The Ich and Qch signals, which were converted to digital, undergo baseband detection by means of a wave detector 4017 using a prescribed system which outputs demodulated data 4018.

[0102] The Ich and Qch signals 4019, which were converted to digital values, are also input into a gain control circuit 4015. The gain of a variable gain circuit is controlled by the gain control circuit 4015 according to the flow chart shown in Fig. 26. In the following the principle of operation of the present invention will be described.

[0103] The received signals input into the radio receiver of the present invention are burst type signals as shown in Fig. 4. These burst type signals are received at a period determined during ordinary reception when TDMA (Time Division Multiple Access) communication is being used. This period can control a variable gain amplifier using information before a burst when sufficiently early compared to the period of the fading. In other words, using an input amplitude value before a burst to determine the gain value of the variable gain amplifier during the present burst makes it possible to

set a level within the dynamic range of the baseband section of a receiver and achieve favorable communication from the start of a burst state.

[0104] Even though this is possible, the electric field strength before a burst and the electric field strength during the present burst will be independent when the burst period is longer compared to the fading period or during an initial connection when beginning communication. Because of this, variable gain amplifier cannot be controlled using the information before a burst and communication cannot be implemented from the first burst. This type of condition has occurred more often in recent years. When taking a small radio receiver into consideration, the drive of a low voltage source such as a dry cell battery is a requisite. And since extending the life of a battery by turning OFF the receiver as much as possible when it is not needed directly leads to longer standby periods, it is an important issue.

[0105] For example, consider when the radio receiver in the composition shown in Fig. 1 is turned ON slightly before the above-mentioned burst signal. Since the received signals are burst type signals, when other users are not using the time before, this time is a non-signal interval. If there are no users using RX1 while using RX2 in Fig. 7, that interval will be a non-signal interval. When there are no signals, the gain of the variable gain amplifier will be at the maximum.

[0106] In order to amplify the received signals by the maximum gain if a burst arrives in this state, the input of the A / D converter will increase beyond the regulated value and become overloaded. Since the control width of the variable gain amplifier is usually about 80 dB, large value of 80 dB, compared to the dynamic range of the A / D converter, will be input when received signals with a large electric field strength are input. In reality, because the high frequency-amplifier block 104, the frequency converter 109, and each block of the baseband amplifier 114 will be saturated, the input of the A / D converter will only have a magnitude of several decibels and the variable gain amplifier must be attenuated 80 dB if this will be at the proper level.

[0107] At this time, the received electric field strength detection section 115 will detect that the input level is large and then attempt to attenuate the variable gain amplifier. Although the reference value supplied by the reference voltage 116 at this time supplies a control target value for the input to the A / D converter, it is preferable to set a value obtained from the maximum input that does not saturate the A / D converter in order to suppress the quantization errors due to the A / D converter to a small level. Normally, a margin is considered and the target value is 70% to 80% of the maximum input. Since the A / D converter is saturated here, the A / D converter outputs a digital value that represents the maximum value. The received electric field strength detection section

115 compares the maximum value to 80% and then controls the variable gain amplifier in response to this difference.

[0108] Although the level seen at the input of the A / D converter is 80 dB larger than the predetermined target value, the level after the A / D converter is at most 1.25 times compared to the target value and the fact that the A / D converter becomes saturated results in many differences with the target value being suppressed. For this reason, there is a possibility of problems of an extremely long time being required to compensate for a level difference of 80 dB and the AGC not converging within one burst but requiring a number of bursts.

[0109] Although the composition of Fig. 1 operated favorably during communication while normal bursts continuously arrived, when an intermittent reception occurred, the receiver turned ON from a non-signal state and the next burst arrived. Therefore, an extremely long time was required for the convergence of the AGC and demodulation of the data within one burst became impossible. Because of this, measures were implemented such as engaging the AGC in advance with the receiver ON for the number of bursts in the non-burst interval that was not required originally. However, since the width of the receiving interval during intermittent reception consumed power, the standby time was one for several cases when only receiving the required intervals.

[0110] In order to solve these problems in this embodiment, a radio receiver will be described using Fig. 26 that can extend the talk time and standby time by means of completing the AGC operation within one arrived burst for bursts which arrive from a non-signal interval, taking levels within the dynamic range of A / D and demodulating signals to achieve a correct output as well as achieve the reception of required bursts only.

[0111] In Fig. 25, the A / D converters 4024, 4025 have a resolution of, for example, 8 bits and the variable gain amplifier is discretely controlled centered on 6 dB. The receiver will turn ON before a few symbols of a receiving interval of an intermittent reception. At this time, the variable gain amplifier is set to the maximum gain by the gain control circuit 4015.

[0112] The gain control circuit controls the variable gain amplifier according to the following procedure. At first, a counter that measures time resets (t = 0) (step 4101). The gain control circuit monitors for any overflow of the A / D converter (step 4102). When there is no overflow, the gain control circuit monitors the maximum value (A / Dmax) of the output of the A / D converter from t = 0 (step 4106). An overflow detection will cause the maximum digital data an A / D converter will output to appear or the A / D converter can be equipped with an overflow detection function that detects an overflow when a flag is raised.

[0113] If an overflow is detected, the variable gain amplifier will be attenuated in four steps (24 dB) (step 4103). Since the variable gain amplifier has analog circuitry, a delay occurs until there is a signal that notifies of attenuation, the attenuation completes, and the signal reaches the gain control circuit. Because the amplitude strength of the attenuated signal cannot be measure correctly during this delay interval, the overflow detection circuit will be halted during the time (t1) interval determined by the value calculated in advance from the delay time. In addition to this, overflow detection will be ignored by the gain control circuit. The overflow detection will restart by resetting (t = 0) the time counter.

[0114] The gain of the variable gain amplifier is determined from the maximum output (A / Dmax) of the A / D converter within time t0 when this operation is repeated and an overflow is not detected between the time (t = t0) set in advance. Here, the range should ideally be 0 dB to 24 dB compared to the maximum output of the A / D converter. Since the A / D converter is an 8-bit converter, the maximum value (A / Dmax) during the t0 interval will be compared to a threshold value 10h (hexadecimal code), 20h, and 40h. When the maximum value (A / Dmax) is smaller that these, the gain will only be 18db, 12 dB, and 6 dB (steps 4110, 4111, and 4112). The procedure will then return to the beginning and perform overflow detection. This operation is repeated until a burst completes (step 4113).

[0115] Here, the gain width that is controlled when an overflow is detected in a range that has a sufficient margin within the dynamic range of the A / D converter when the maximum output of the A / D converter is attenuated from the dynamic range of the A / D converter. The gain width is restricted as much as possible to large values. For an 8-bit converter, the gain will be 24 dB considering up to approximately the lower 4 bits.

[0116] According to the above-mentioned method, because an overflow is detected and the gain lowered a great extent, time within the dynamic range of the A / D is dramatically shortened. In addition, since it is possible to calculate whether an optimum level is reached if the gain is controlled to a certain degree once entering within the dynamic range, the convergence will not require that much time. Also, since the gain control width was found from an RSSI calculated by means of conventional digital signal processing, delays occurred due to the calculation time, average time, and comparison time. In this embodiment however, since the detection of an A / D overflow will immediately control the gain to 24 dB, a high-speed draw can be realized.

[0117] According to the description above, an input with a large amplitude of 80 dB can be used for the A / D and an optimum input level can be achieved during a time of approximately four times the delay amount d from the variable gain amplifier. Since the delay amount d is normally 1 to several μsec, the initial draw operation of

the AGC can almost be completed at several symbols to several tens of symbols during communication with transmission speeds of several 10 to several 100 kHz. This makes it possible to complete the initial operation of the AGC at the top of one burst, correctly demodulate subsequent signals, and then output the data during the arrival of a receiving burst from a non-signal state such as an intermittent reception. Normally, since a synchronizing preamble signal is arranged for several tens of symbols from the top during this type of intermittent reception, there is no influence on the transfer of data.

[0118] When there is attenuation from an overflow in this embodiment, the attenuation amount will increase eliminating the overflow for a fixed period of time. Then, after recognizing that the overflow is within the dynamic range of the A / D, the gain increases with a small width thereby making it possible to achieve a high-speed and accurate AGC.

[0119] Although the width of the variable gain amplifier was discretely controlled in the example above, the width when increasing the gain can be continuously controlled or a high-speed operation can be performed in the same manner.

[0120] Fig. 27 shows another embodiment of a radio receiver. In this figure, the overflow of the above-mentioned A / D converter is controlled by 4201. If the level is adjusted to a suitable range by means of an AGC operation due to the overflow of the A / D converter,

correct data will be output. Several synchronizations such as a TDMA synchronization will be established by this. Once an overflow is detected, the AGC will be attenuated to 24 dB due to the overflow of the A / D converter. Therefore, this is not stable compared to the method shown in Fig. 1 using an ordinary continuous burst. Furthermore, the stability will be improved even more using RSSI detection for signals which pass through the filter 4203 without an output of the A / D converter as is. Because a TDMA synchronization was established, a normal level will be judged and the control of the width will be switched to the second gain control circuit 4202 that is stable even if a late delay exists. This makes it possible to realize an AGC circuit that is stable even during received signal demodulation and also allows the receiving error rate during intermittent reception to be exceptionally improved. Fig. 27 (b) shows the detailed composition of the second gain control circuit 4202. This circuit finds the envelope of the received signals, finds the difference between the envelope amplitude value and a reference value (Ref), finds the time average, and then determines the control width.

[0121] Fig. 28 shows another embodiment of a radio receiver. Here, an application to a receiver that automatically controls the frequency (AFC) using digital signal processing will be described. In this embodiment the composition is such AFC is applied from the output of the demodulator 4302. Although an AFC that uses digital

signal processing finds a frequency control width from the digital signals input from the A / D converter, the probability that a malfunction will occur in the AFC operation during an interval when the AGC is not converging will become very high. The AFC operation is preferably halted when there are no signals. In this embodiment, the AFC halts in an initial state and the control frequency is either taken before the communication or the control frequency is defined as a default. In the same manner as Fig. 28, the AGC operation due to an overflow of the A / D converter is performed, the input to the A / D converter is judged to be a normal level based on the establishment of the TDMA synchronization, and then the AFC operation starts. According to this type of operation, malfunctions of the AFC can be prevented thereby making it possible to perform stable, high-quality communication.

[0122]

[Effect of the Invention] According to the present invention, high-speed variable gain control can be performed without losing the dynamic range when there are rapid fluctuations of the input amplitude.

[Brief Description of the Drawings]

[Fig. 1] describes the radio receiver according to the present invention.

[Fig. 2] shows the composition of a radio receiver that controls gain using digital signals.

[Fig. 3] shows an example of a method to realize a frequency converter.

[Fig. 4] describes high-speed fading.

[Fig. 5] describes low-speed fading.

[Fig. 6] describes a receiving level diagram.

[Fig. 7] describes the composition of a reception frame and a slot.

[Fig. 8] describes a method to calculate received electric field strength.

[Fig. 9] describes a method to initialize a receiving mode.

[Fig. 10] describes an empty channel search.

[Fig. 11] describes a method to set a receiving mode.

[Fig. 12] describes the composition of a slot.

[Fig. 13] describes a method to set another receiving mode.

[Fig. 14] describes a receiving level diagram when adjusting the gain of a receiver section.

[Fig. 15] describes a method to adjust the gain of a receiver section.

[Fig. 16] describes a method to set another receiving mode.

[Fig. 17] shows the composition of the AGC amplifier of the present invention.

[Fig. 18] shows the composition of a level detection circuit in a conventionally used baseband.

[Fig. 19] shows the composition of a radio receiver with a newly added level detection circuit.

[Fig. 20] shows the second composition of a radio receiver with a newly added level detection circuit.

[Fig. 21] describes the operation of a new level detection circuit.

[Fig. 22] shows the composition of a new baseband delayed wave detection circuit.

[Fig. 23] shows an example of the composition of a radio receiver using a new AGC circuit.

[Fig. 24] shows the third composition of the radio receiver with a newly added level detection circuit.

[Fig. 25] shows the composition of a radio receiver according to another gain control system.

[Fig. 26] shows the control procedure of another gain control system.

[Fig. 27] shows the composition of a radio receiver according to another gain control system.

[Fig. 28] shows the composition of a radio receiver according to another gain control system.

[Fig. 29] describes the principle of operation of a conventional direct conversion receiver.

[Fig. 30] describes a gain control system using a high-frequency amplifier.

[Fig. 31] describes a gain control system using a high-frequency amplifier and a baseband amplifier.

[Fig. 32] describes a gain control system using a digital signal process.

[Fig. 33] describes a gain control system using a limiter.

[Explanation of the Reference Numerals]

101 -- Receiving antenna

102 -- High-frequency amplifier of the initial stage

103 -- High-frequency amplifier of the latter stage

104 - High-frequency amplifier block

105 -- Local oscillator

106 - π/2 phase converter

107, 108 -- Frequency converter

109 -- Frequency converter pair

110, 111 -- Baseband filters

112, 113 -- Baseband amplifiers

114 -- Baseband amplifier pair

115 -- Received electric field strength detection and comparison circuit

116 -- Reference voltage

117 -- Wave detector

118 -- Demodulation signal

119 -- IQ signal

120 -- Gain control signal to baseband amplifier

121 -- Gain control signal to frequency converter

122 -- Gain control signal to high-frequency amplifier

123 -- Gain control signal

124, 125 -- A / D converter

201 -- Receiving antenna

202 -- RF filter

203 -- High-frequency amplifier

204 -- Frequency converter

205 -- π/2 phase converter

206, 207 -- Local oscillators

208, 209 -- AC couplers

210, 211 - Low-pass filters

212, 213 -- Baseband amplifiers

214 -- Wave detector

301 -- Receiving antenna

302 -- High-frequency amplifier

303 -- RF filter

304, 312 -- Frequency converters

305, 313 -- Local oscillators

306 -- Intermediate frequency (channel selection) filter

307 -- AGC amplifier

308 -- Voltage detection and comparison circuit

309 -- Reference voltage

310 -- Demodulation circuit

311 -- AGC control signal

401 -- Receiving antenna

402 -- High-frequency amplifier

403, 404 -- Frequency converters

405 -- Local oscillator

406 - π/2 phase converter

407, 408 -- A / D converters

409, 410 -- Channel select filters

411 -- Digital gain control and wave detect section

412 -- Digital signal processing section

501 -- Receiving antenna

502 -- High-frequency amplifier

503, 504 -- Frequency converters for quadrature demodulation

505, 511 -- Local oscillators

506, 512 -- π/2 phase converter

507, 508 -- Baseband channel select filters

509, 510 -- Frequency converter for quadrature modulation

513 - Adder

514 - Limiter

515 -- Demodulator

601 -- Receiving antenna

602 -- High-frequency amplifier

603, 604 --Frequency converters for quadrature demodulation

605 -- Local oscillator

606 -- π/2 phase converter

607, 608 -- Baseband channel select filters

609, 610 -- Baseband amplifiers

611, 612 -- A / D converters

613 -- Digital gain control and detection section

614 -- Gain control signal

701 -- Receiving antenna

702 -- High-frequency amplifier

703, 704 -- Frequency converter for quadrature demodulation

705 -- Local oscillator

706 -- π/2 phase converter

707, 708 -- Baseband channel select filters

709, 710 -- Baseband amplifiers

711, 712 -- A / D converters

713 -- Digital gain control and detection section

714 -- Gain control signal to baseband amplifier

715 -- Gain control signal to high-frequency amplifier

1401, 1402 -- Frequency converters

1403 -- Frequency converter pair

1404 - Amplifier

1405 -- Local oscillator

1406 -- Saturation portion

1407 -- Linear portion

1408 -- Gain control signal

1409 -- Control circuit

1501, 1506 - Frames

1502, 1507 -- Slots

1503, 1508 -- Requested receiving slots

1504, 1509 -- Subsequent receiving slots

1505, 1510 -- All other slots

1601 -- Requested receiving slot

1602 - Preceding receiving slot

1603 -- Subsequent receiving slot

1604, 1605 -- Guard time

1606 -- Start symbol

1607 -- Preamble

1608 -- Identification word

1609 -- Information signal

1701 -- Received electric field strength during high-speed fading

1702 - Length of one slot length

1703, 1704 -- Requested receiving slots

1705 --- One frame length

1801 -- Received electric field strength during low-speed fading

1802 -- One slot length

1803, 1804 -- Requested receiving slots

1805 --- One frame length

2001, 2101 -- Receiving antennas

2002, 2102 -- High-frequency amplifiers

2003, 2103 -- Frequency converters

2004, 2104 -- Baseband amplifiers

2005, 2105 -- A / D converters

2006 -- Received input level

2007 -- Gain of the high-frequency amplifier

2008 -- Gain of frequency converter

2009 -- Gain of baseband amplifier

2010 -- Output level of baseband amplifier (A / D converter input level)

2106 -- Baseband amplifier output (A / D converter input) level before gain adjustment

2107 -- Baseband amplifier output (A / D converter input) level after gain adjustment

2108 -- Receiving level diagram before gain adjustment

2109 -- Receiving level diagram after gain adjustment

2110 -- Input range of A / D converter

2111 -- Maximum input of A / D converter

2112 -- Minimum input of A / D converter

3001 -- Radio receiver section

3002, 3003 -- AD converters

3004 -- Wave detector

3005 -- Decision circuit

3006 -- Phase detection circuit

3007 -- Level detection circuit

3011, 3012 -- Sampling circuits

3013 -- Phase detection circuit

3014 -- Rotational converter

3101, 3102 -- A / D converters

3103, 3104 -- Delay device

3106 -- Adder

3107 -- Subtractor

3200 to 3203 -- Point where wave detection output was sampled using a symbol rate

3301, 3302 -- Baseband amplifiers

3303, 3304 -- AD converters

3305 -- Delayed wave detection circuit

3306, 3307 -- Sampling circuits

3308 -- Decision circuit

3309 -- Level detection circuit

3310 -- Difference circuit

3311 -- Integration circuit

3312 -- Conversion circuit

3501, 3502 -- A / D converters

3503 -- Delayed wave detection circuit

3504 -- Decision circuit, serial - parallel converter

3505 to 3508 -- Sampling circuits

3509, 3510 -- Absolute value conversion circuits

3511 -- Adder

3512 -- Constant multiplier

4001 -- Receiving antenna

4004 -- High-frequency amplifier

4005 -- Local transmitter

4006 -- π/2 phase converter

4007, 4008 -- Frequency converter

4009 -- Frequency converter pair

4010, 4011 -- Baseband filters

4012, 4013 -- Baseband amplifiers

4014 -- Baseband amplifier pair

4124, 4125 -- A / D converters

4017 -- Demodulator (wave detector)

4018 -- Demodulated data

4019 -- Baseband digital signal

4015 -- Gain control circuit

4203 -- Digital filter

4210 -- Gain control circuit using A / D overflow detection

4202 -- Gain control circuit using RSSI

4301 -- AFC control circuit

4302 -- Demodulator (wave detector)

Fig. 1

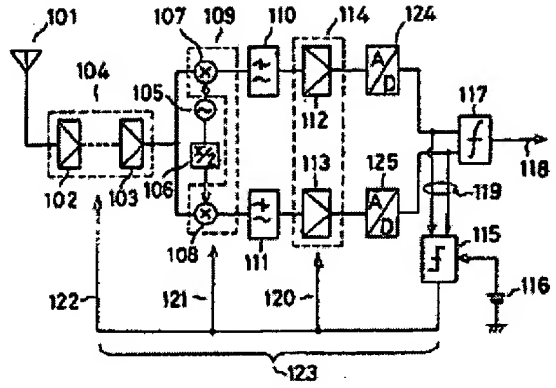
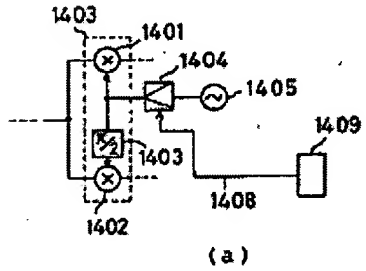
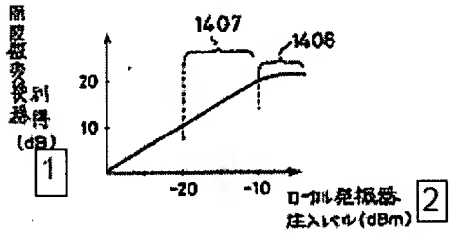


Fig. 3



(a)

Fig. 3 (b)



(b)

Key: a) Frequency converter gain (dB); b) Local oscillator injection level (dBm)

Fig. 4

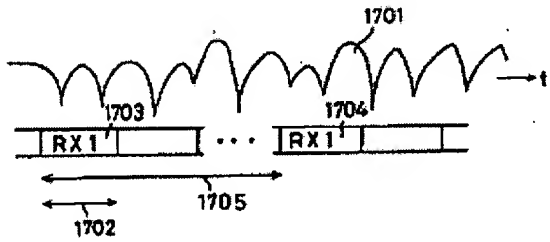


Fig. 5

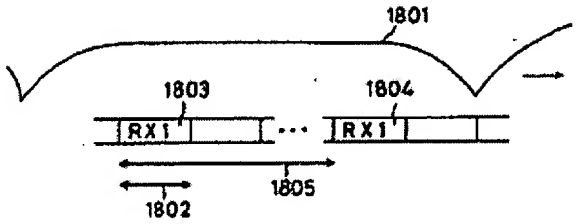


Fig. 2

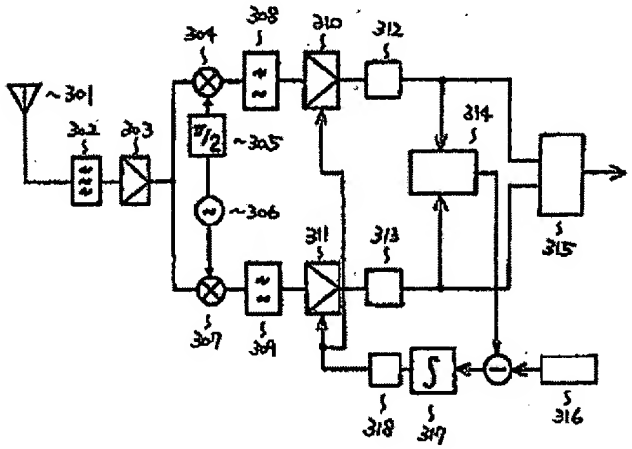
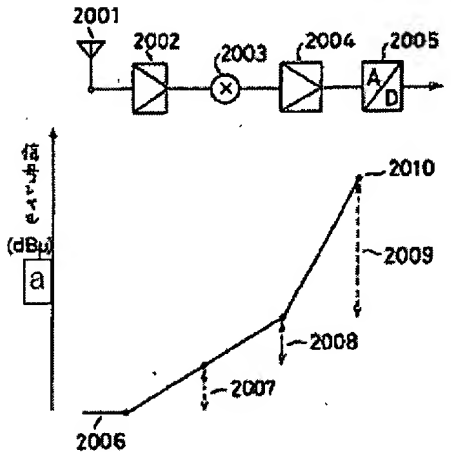


Fig. 6



Key: a) Signal level (dBμ)

Fig. 7

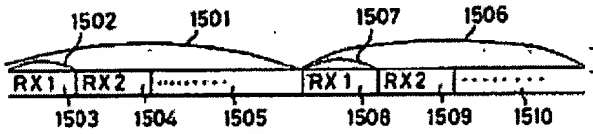


Fig. 10

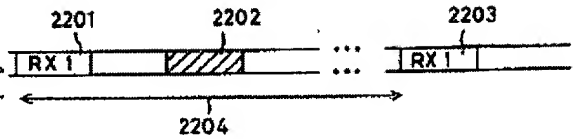


Fig. 12

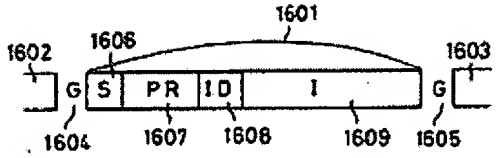
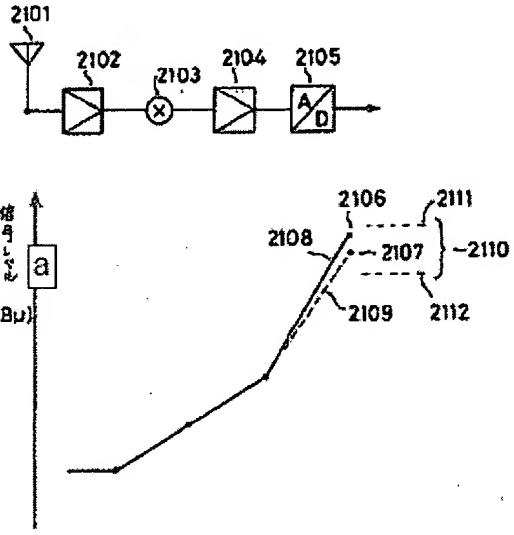


Fig. 14



Key: a) Signal level (dBμ)

Fig. 18

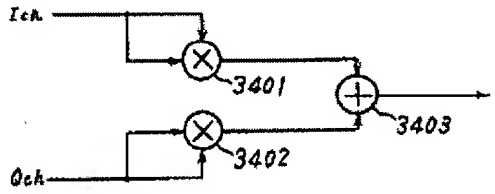
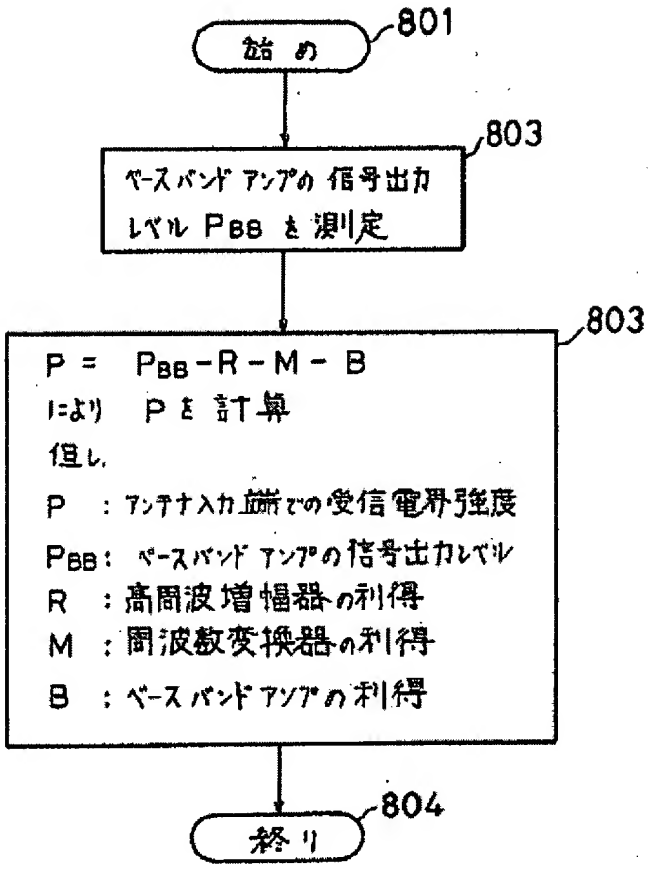


Fig. 8



801 Start
803 Measure signal output level PBB of baseband amplifier
803 Calculate P using P = PBB - R - M- B
P: Received electric field strength at antenna input terminal
PBB: Signal output level of baseband amplifier
R: Gain of high-frequency amplifier
M: Gain of frequency converter
B: Gain of baseband amplifier
804 End

/20

Fig. 19

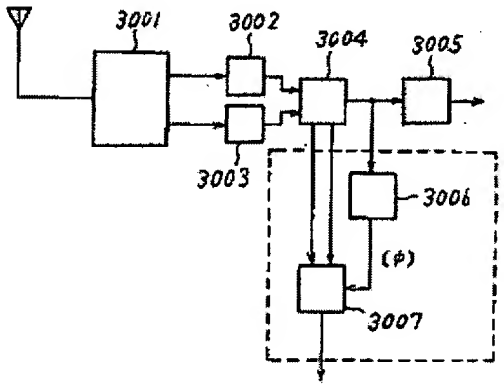


Fig. 29

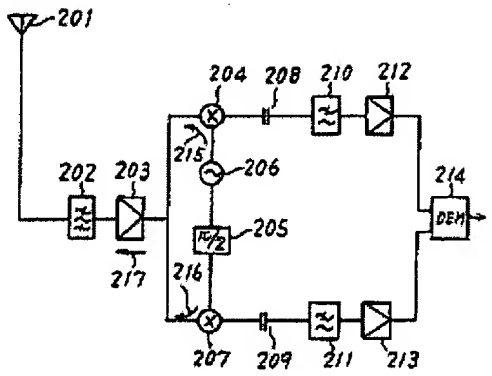


Fig. 17

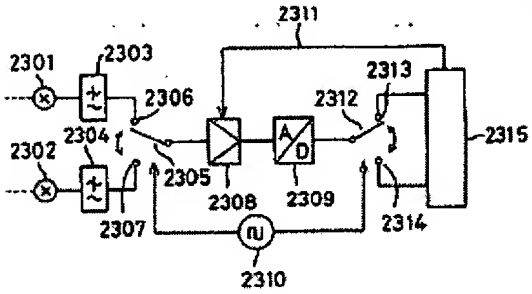


Fig. 20

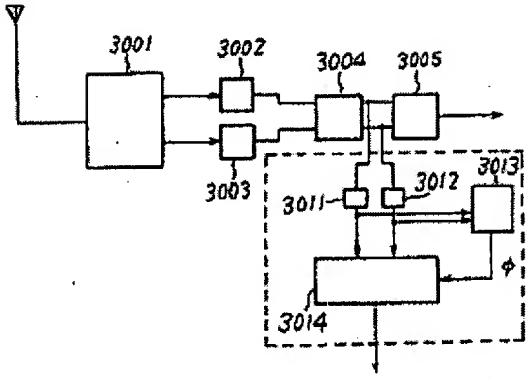
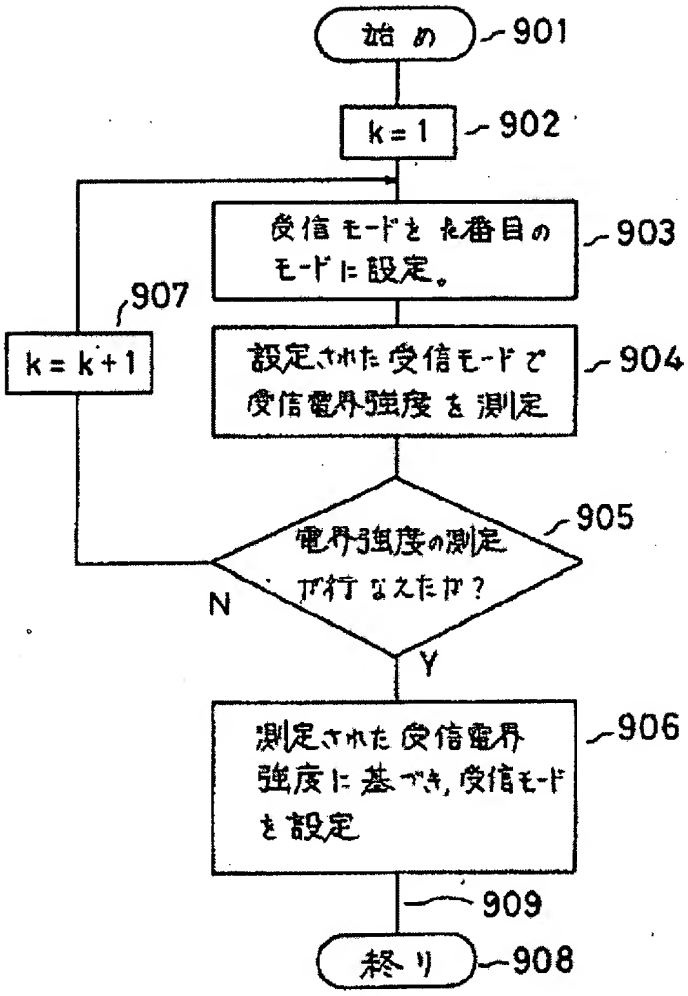


Fig. 9



901 Start

903 Set receiving mode to No. k mode

904 Measure received electric field strength in set receiving mode

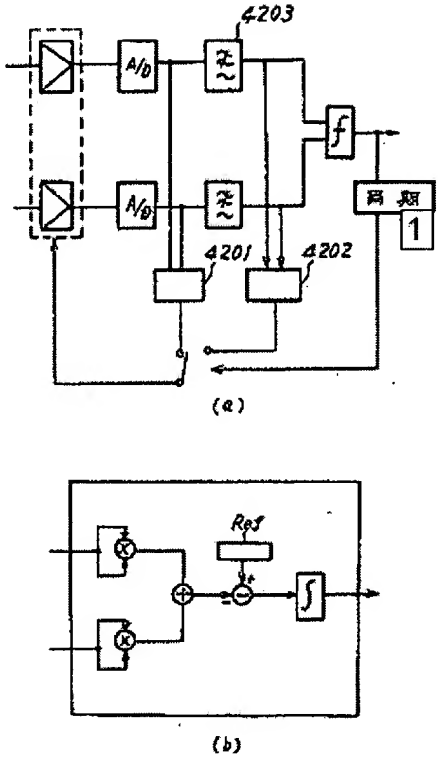
905 Was electric field strength measured?

906 Set receiving mode based on the measured received electric field strength

908 End

/21

Fig. 27



Key: 1) Synchronized.

Fig. 22

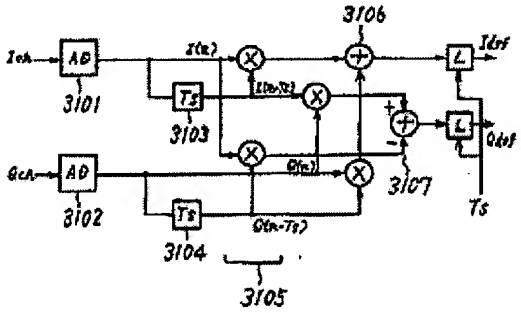
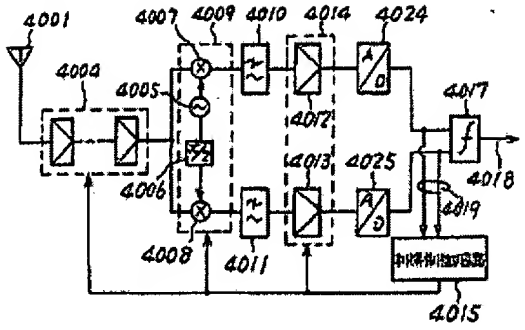
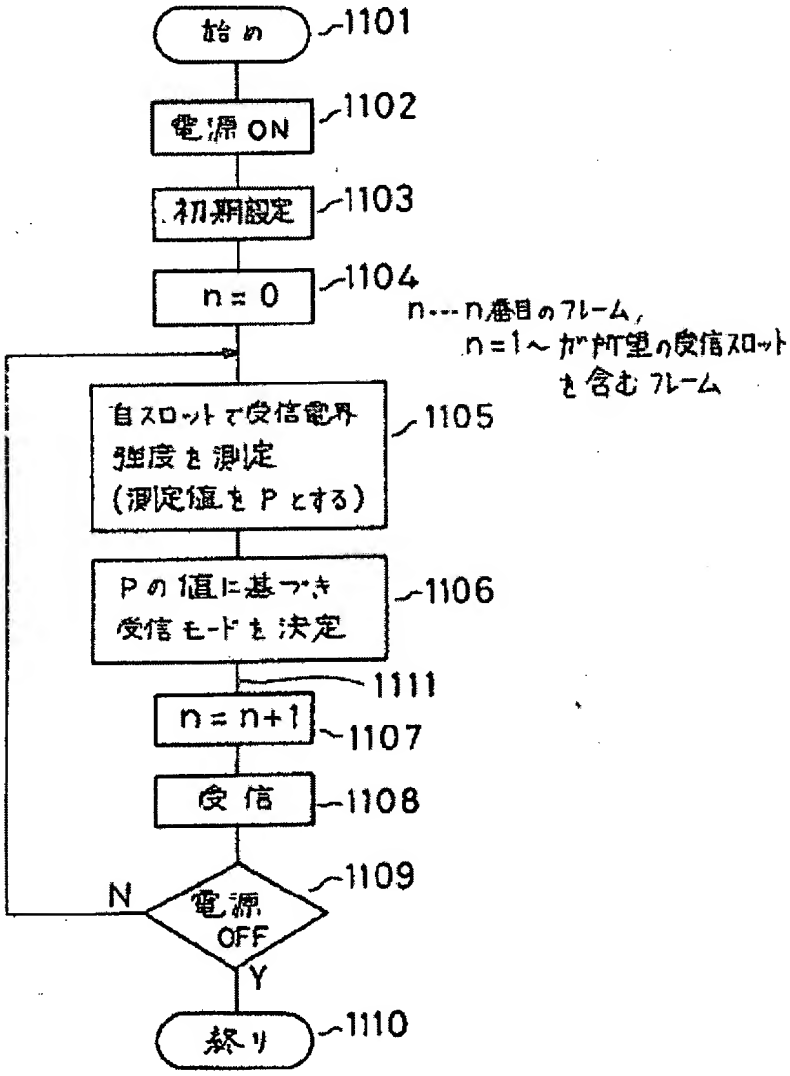


Fig. 25



4015 Gain control circuit

Fig. 11



1101 Start
1102 Power ON
1103 Initial settings
1104 n = 0

n --- nth frame
n = 1 ~ Frame containing requested receiving slot

1105 Measure received electric field strength at own slot (measured value is P)

1106 Determine receiving mode based on value of P

1108 Receive

1109 Power OFF

1110 End

Fig. 30

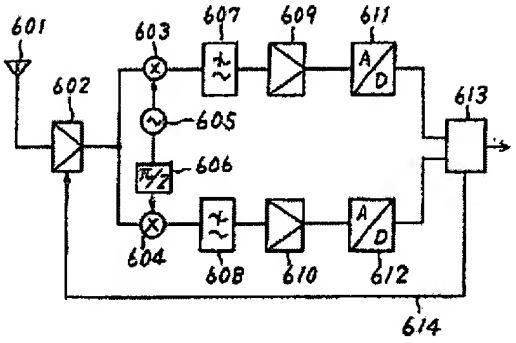


Fig. 31

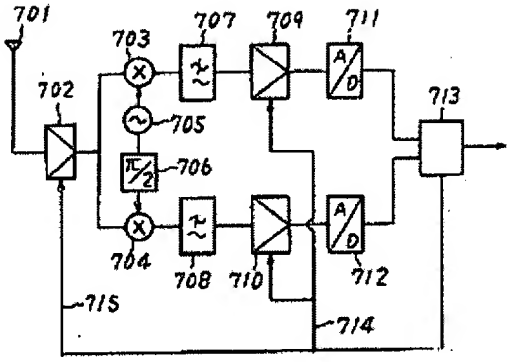
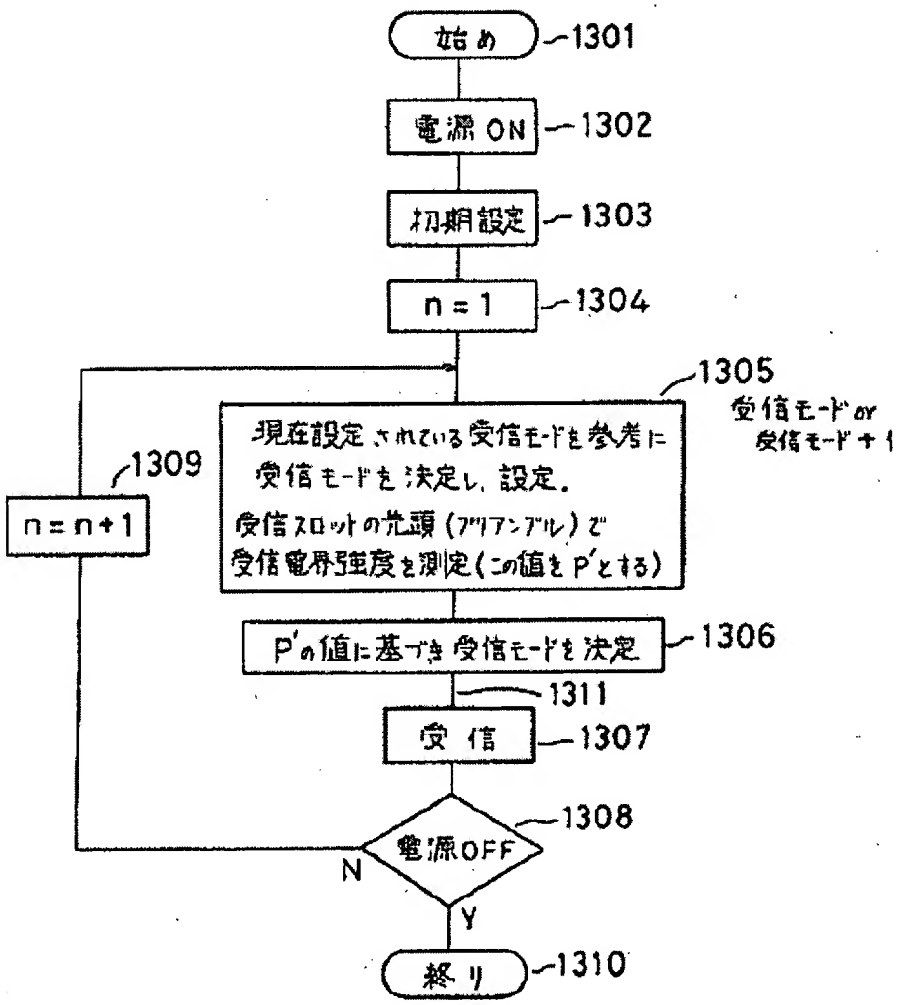


Fig. 13



1301 Start
1302 Power ON
1303 Initial settings

1305 Receiving mode or receiving mode + 1
[Determine and set receiving mode referring to the currently set receiving mode. Measure received electric field strength at top (pre-amplifier) of receiving slot.]
1306 Determine receiving mode based on value of P'
1307 Receive
1308 Power OFF
1310 End

Fig. 32

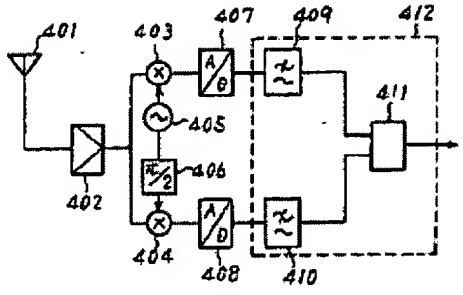


Fig. 33

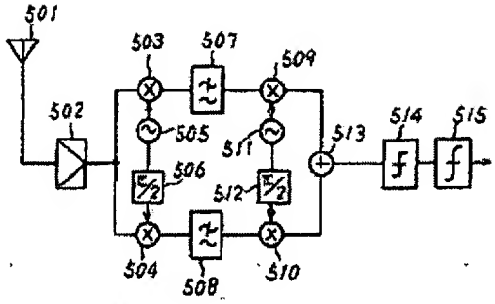
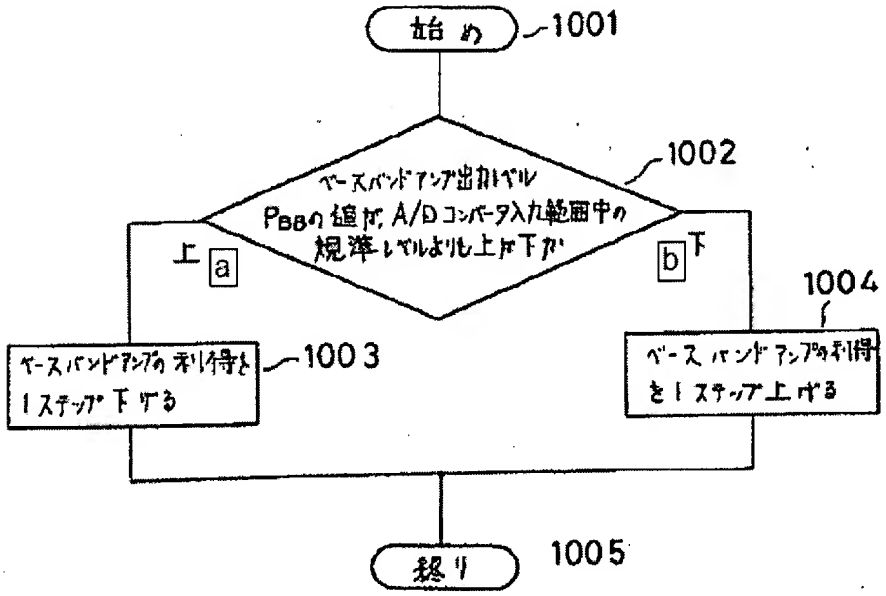


Fig. 15



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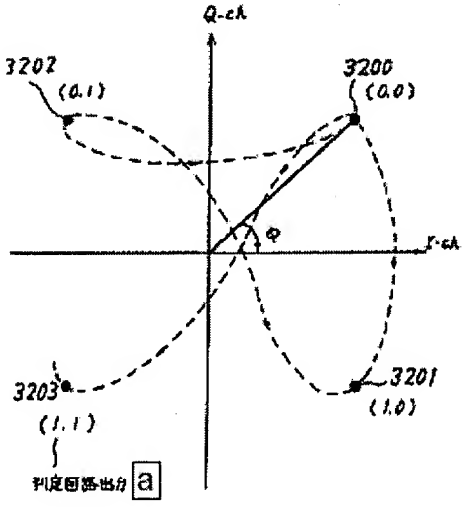
1001 Start
1002 Is the value of baseband amplifier output level PBB higher or lower than the reference level within the A / D converter input range?
a) Higher
1003 Lower gain of baseband amplifier one step
b) Lower
1004 Raise gain of baseband amplifier one step
1005 End

Fig. 21



Key:
a) Decision circuit output

Fig. 23

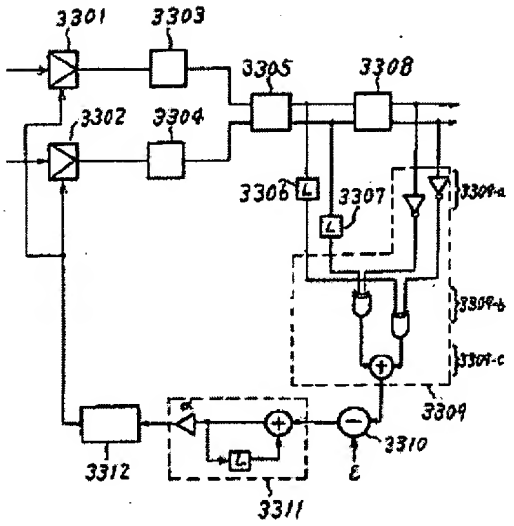
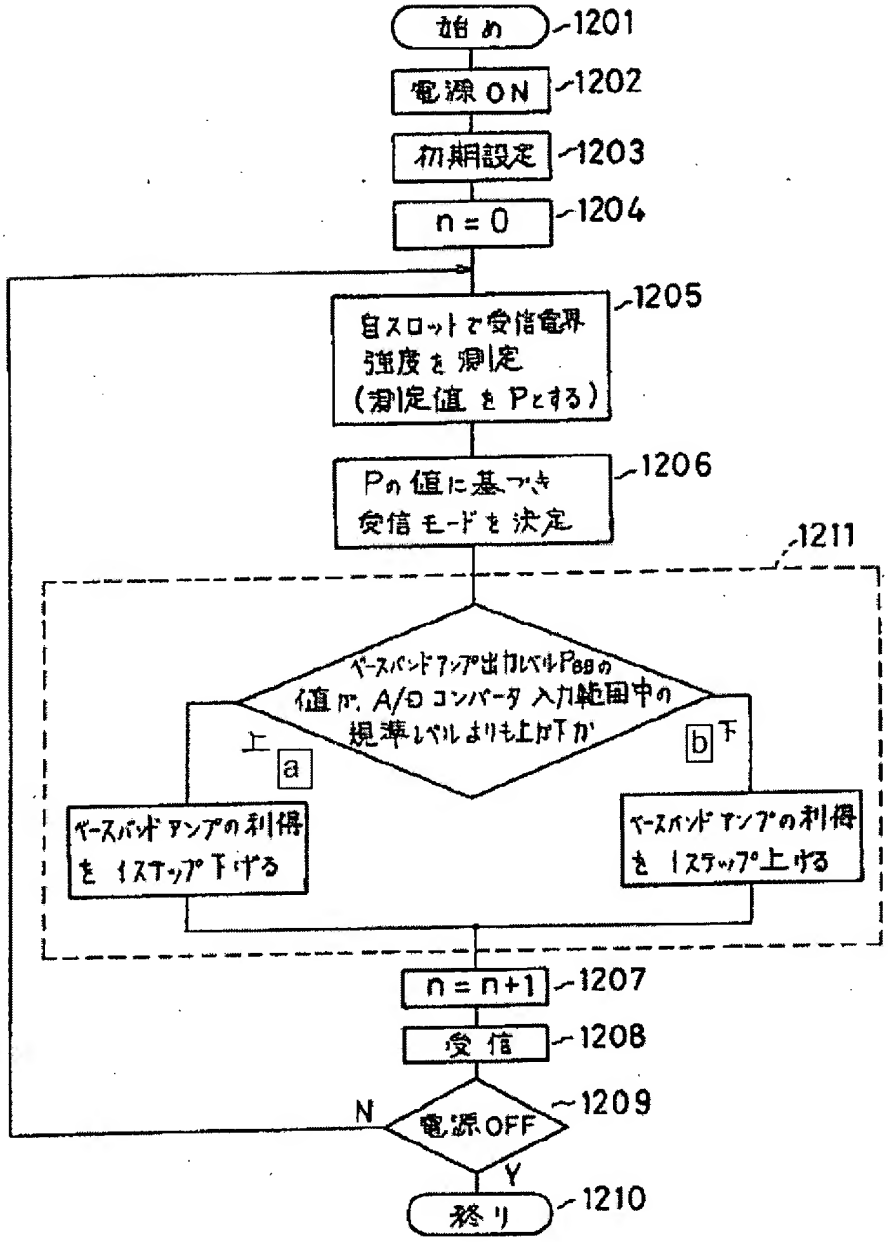

3301
3303
3305
3308
3302
3304
3306
3307
3309-a
3309-b
3309-c
3309
3310
3312
3311
ε

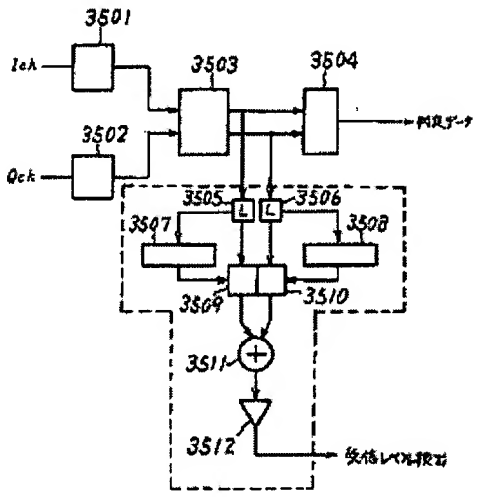
Fig. 16



1201 Start
1202 Power ON
1203 Initial settings
1205 Measure received electric field strength at own slot (measured value is P)
1206 Determine receiving mode based on value of P
1211 Is the value of baseband amplifier output level PBB higher or lower than the reference level within the A / D converter input range?
a) Higher

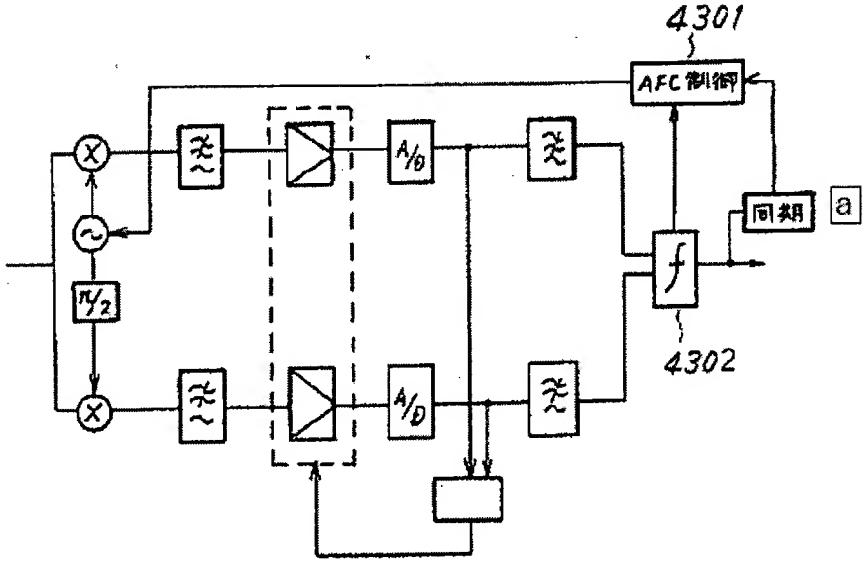
Lower gain of baseband amplifier one step
b) Lower
Raise gain of baseband amplifier one step
1208 Receive
1209 Power OFF
1210 End

Fig. 24



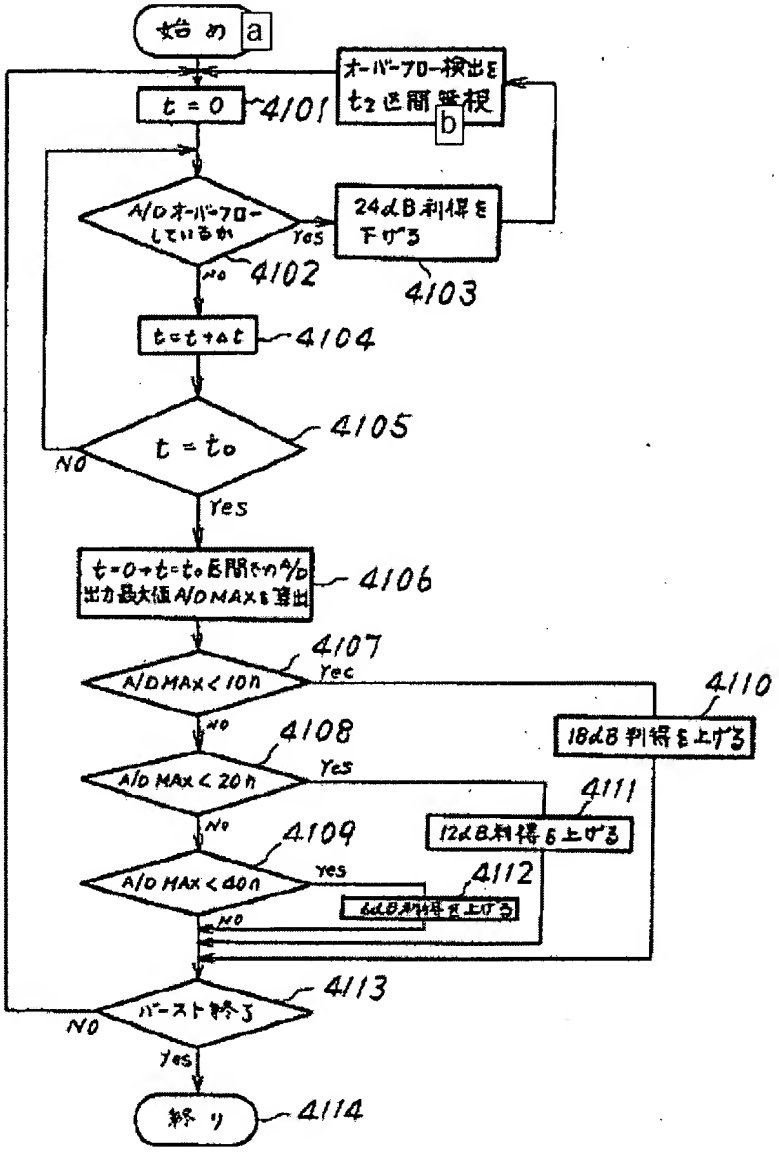
3504 Judgment data
3512 Detect receiving level

Fig. 28



4301 AFC control
a) Synchronized

Fig. 26



a) Start
b) Overflow detection ignores t2 interval
4102 Is there A / D overflow?
4103 Lower gain 24 dB
4106 Calculate A/ D output maximum value A /Dmax during t = 0 - t = to interval
4110 Raise gain 18 dB
4111 Raise gain 12 dB
4112 Raise gain 6 dB
4113 End burst
4114 End